16 Channel logic scope
16 Kanal logik-Oszilloskop
Oscilloscope logique 16 voies
PM3540

Instruction manual - Gerätehandbuch - Notice d'emploi et d'entretien

9499 503 00402
800701

S&i
Scientific & Industrial equipment division

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Gebrauchsanleitung

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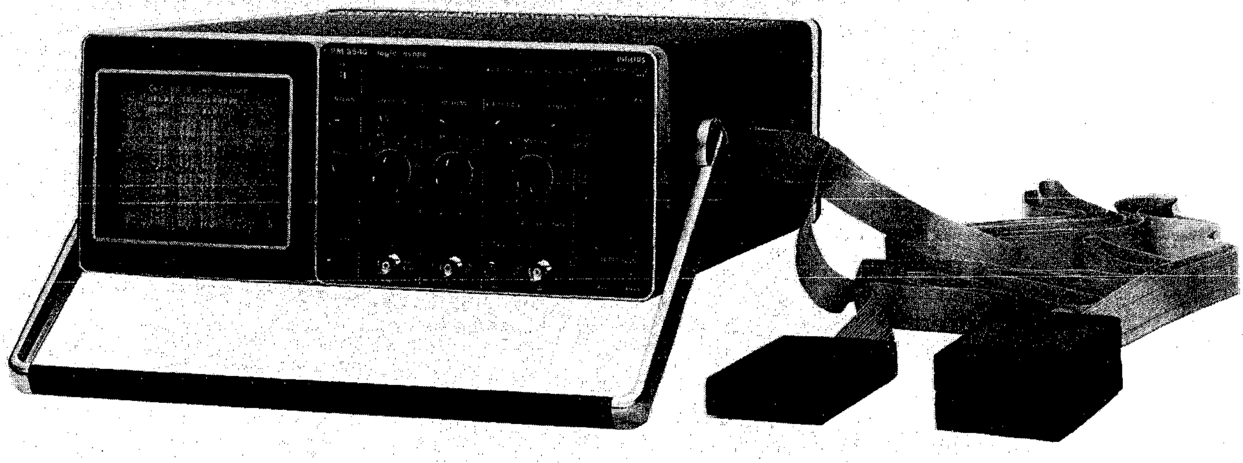

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IMPORTANT

In correspondence concerning this instrument, please quote the type number and serial number as given on the type plate.

WICHTIG

Bei Schriftwechsel über dieses Gerät wird gebeten, die genaue Typenbezeichnung und die Gerätenummer anzugeben. Diese befinden sich auf dem Leistungsschild.

IMPORTANT

RECHANGE DES PIECES DETACHEES (Réparations)

Dans votre correspondance et dans vos réclamations se rapportant à cet appareil, veuillez **TOUJOURS** indiquer le numéro de type et le numéro de série qui sont marqués sur la plaquette de caractéristiques.

Note:	*The design of this instrument is subject to continuous development and improvement. Consequently, this instrument may incorporate minor changes in detail from the information contained in this manual.*
Bemerkung:	*Die Konstruktion und Schaltung dieses Geräts wird ständig weiterentwickelt und verbessert. Deswegen kann dieses Gerät von den in dieser Anleitung stehenden Angaben abweichen.*
Remarques:	*Cet appreil est l'objet de développements et améliorations continuels. En conséquence, certains détails mineurs peuvent différer des informations données dans la présente notice d'emploi et d'entretien.*

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1. General Information

1.1. INTRODUCTION

The PM 3540 logic-scope is a compact, portable instrument, featuring ergonomic design and extensive measurement capabilities. The logic-scope is a combination of a high-performance 16 channel logic state analyzer and a sophisticated 35 MHz dual-trace oscilloscope. Due to this combination, the instrument has the capability of testing all different types of computer-based systems, in both the data and timing domain.
In data domain the analyzer allows the user to monitor the software, as to where the fault is located.
In timing domain the oscilloscope enables the user to indicate timing problems, as to what causes the fault (hardware faults).
These analyzer-oscilloscope functions, combined in one stand-alone test-instrument makes it ideal for a wide range of use in research, development, production testing, trouble shooting, maintenance, field-service and educational applications.
A cathode-ray tube with a useful screen area calibrated into 8x10 divisions by an internal graticule, displays in the oscilloscope mode two well-defined traces. In the analyser mode, tabular data formats can be displayed in binary, octal or hexadecimal form.
A double-insulated power supply allows the frame ground to be directly connected to floating ground circuits, provided this ground does not carry live potentials.

Interference by ground currents, as is frequently experienced with grounded instruments, is also substantially reduced.

Use of the logic-scope in the field is further facilitated by optional battery operation.

WARNING: The frame ground (and the probe's ground lead) must not be connected to live potentials.

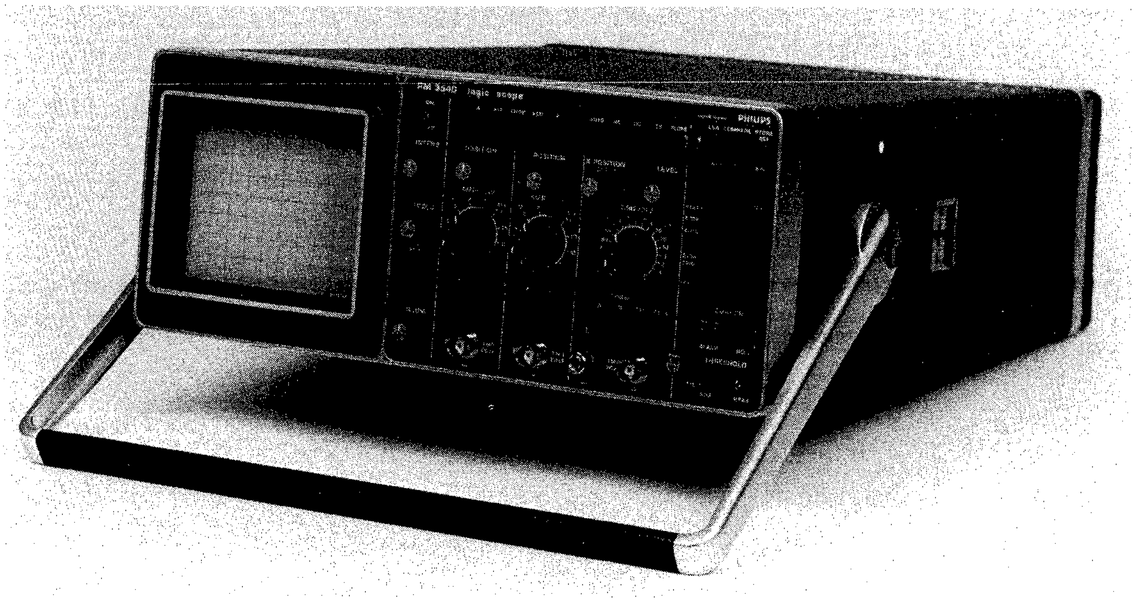


Fig. 1.1. Logic-scope PM 3540

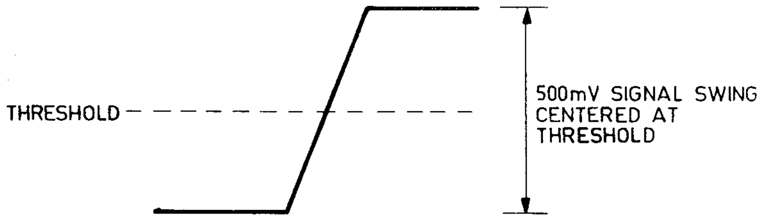

THRESHOLD
500mV SIGNAL SWING CENTERED AT THRESHOLD

Fig. 1.2. Minimal signal swing

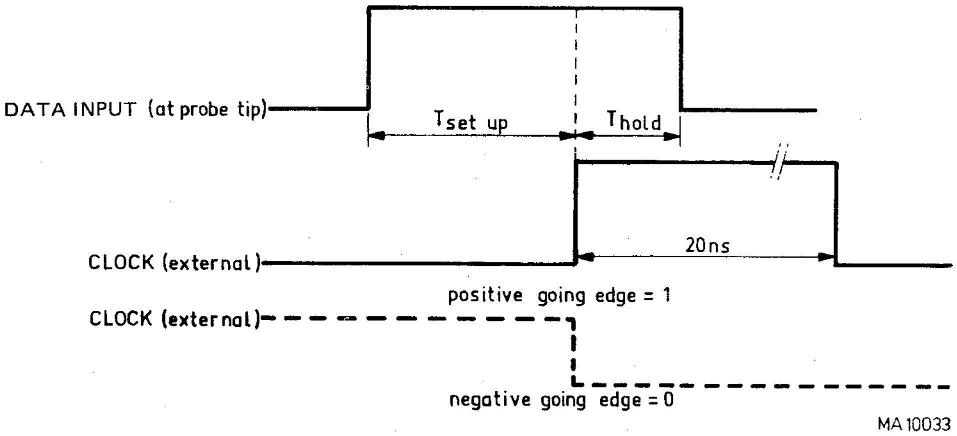

DATA INPUT (at probe tip)
$T_{set\ up}$
T_{hold}
CLOCK (external)
20ns
positive going edge = 1
CLOCK (external)
negative going edge = 0
MA 10033

Fig. 1.3. Definition of set-up and hold times

1.2. CHARACTERISTICS

This instrument has been designed and tested according to IEC Publication 348 for Class II instruments and has been supplied in a safe condition. The present Instruction Manual contains information and warnings which should be followed by the purchaser to ensure safe operation and to maintain the instrument in a safe condition.

Properties expressed in numerical values with stated tolerances are guaranteed for ambient temperatures of +5 °C ... +40 °C unless stated otherwise. Numerical values without tolerances are typical and represent the characteristics of an average instrument. This specification is valid after the instrument has warmed up for 15 minutes.

OPERATION MODES : – Logic State Analyzer only
– Oscilloscope only
– Both Logic State Analyzer and Oscilloscope where L.A. triggers the scope.

NOTE : For operation and selection procedures about these modes, see Chapter 2 "DIRECTIONS FOR USE".

1.2.1. Characteristics of the analyzer part

1.2.1.1. Analyzer inputs : 3 Multi-lead input sockets providing:
– 16 data channels (via 2 sockets)
– 1 Clock
– 3 Clock qualifiers } (via 1 socket)

1.2.1.2. Data input : Via 3 multi-lead probe Pod's PM 8820 providing connections for 8 inputs each:

All values are typical values and specified at the probe tip(s)

– Probe 1, channels 0 ... 7
– Probe 2, channels 8 ... 16
– Probe 3, clock and qualifiers

Impedance : 4 MΩ//6 pF

Max. Voltage : –50 V ... +50 V

Threshold : TTL, +1,4 V fixed
Variable: From 0 to +10 V continuously adjustable via front panel measuring output socket.

Max. sensitivity : 500 mV p-p signal swing (see Fig. 1.2.).

Set-up and hold time: : Set-up time = 40 nsec.
Hold time = 20 nsec.,
with respect to the external active clock edge (see Fig. 1.3.).

1.2.1.3. Clock

Source : External (synchronous), input via probe Pod PM 8820.

Threshold : Same specification as data input

Clock rate : Max. 10 MHz.

Clockpulse width : Min. 20 nsec. (see Fig. 1.3.).

Sampling : Selectable on positive or negative clock edge.

1.2.1.4. Clock qualifier

Number : 3 clock qualifiers (input via multi-lead probe PM 8820).

Threshold : Same specification as data input.

Sampling : Only occurs when qualifier is "true" at clock edge.

"True" selection : "1" for high
"0" for low
"X" for don't care (qualifier not in use).

Set up and hold time : Set up time = 20 nsec.
Hold time = 5 nsec.,
with respect to the external active clock edge (see Fig. 1.3.).

1.2.1.5. *Trigger*

Source : Internal, external, mixed and manual

Internal : By trigger word recognition on 16 channels.

External : Input via front panel BNC socket "EXTERNAL" in the QUAL mode. Triggering only occurs, when trigger input is "true" at clock edge and trigger word is set at don't care (X ... X).
"True" is, when input signal is above threshold level but minimum TTL level.

Mixed : By trigger word recognition on 16 channels together with the trigger qualifier, which is a signal supplied externally.
The trigger qualifier is input via the front panel BNC socket "EXTERNAL" in the QUAL mode.
Trigger qualifier input must be "true" at clock edge.
"True" is, when input signal is above threshold level but minimum TTL level.

Manual : Via front panel START/STOP pushbutton switch.

Trigger word selection :
- By specifying directly from the captured data with operating STORE TRIG pushbutton switch, contents of the first word of the displayed format will become new trigger word (see Fig. 2.5.).
- By selection via CRT display, cursor and controls 1/+, X and 0/– in the required formats (Hex, Oct, or Bin).

Triggering delay : Triggering can be delayed by 0...9999 clock pulses to be selected via CRT and selection pushbuttons + and –.
Trigger delay on/off switching by pushbutton.

1.2.1.6. *Start*

Source : Automatic or manual

Automatic : The instrument starts itself automatically after a display time of approximately 1 second to allow pseudo real time observations.

Manual : Via front panel START/STOP pushbutton switch.

1.2.1.7. *Memory*

: The memory format is 64x16 bit words.
In the compare mode a second memory of the same size is used.

1.2.1.8. *Display (see also Fig. 2.5.)*

:
- CRT of oscilloscope (see 1.2.2.1. for characteristics).
- In the top part of the screen a continuous heading is given containing the parameters and the status of the instrument.
- Line number indication.
  Trigger word is indicated as TRIG and is line number 0. All other lines are measured relatively to the trigger word.
  Also in the delay mode.
- Cursor (in heading) horizontally and vertically positionable.
- Column Blank and Line Roll facilities.

Display modes : State table format in binary, hexadecimal or octal.
In binary the state table is displayed in 16 words of 16 bits. The 16 bits are divided in 4 groups of 4 bits.
In the hexadecimal and octal modes the state table and trigger word are regrouped.

1.2.2. Characteristics of the oscilloscope part

Including the combined analyzer/oscilloscope functions with the trigger sources:

- Y_A, Y_B, Composite and External (via oscilloscope)
- Data and Qual (via analyzer).

	Designation	*Specification*	*Additional Information*
1.2.2.1.	*C.R.T.*		
	Type	D14-125 GH	Rectangular mesh-type
	Measuring area	8x10 divisions	1 div. equals 1 cm with 2 mm subdivisions along the central axes.
	Screen type	P31 (GH)	P31 (GM) and P7 (GM) optional
	Total acceleration voltage	10 kV	
	Graticule	Internal	Cont. variable illumination
1.2.2.2.	*Vertical amplifier*		
	Display modes	Channel A only	
		Channel B only	
		A and B chopped	Chopped at approx. 500 kHz
		A and B alternated	
		A and B added	
	Channel B polarity	Normal or inverted	
	Response:		
	Frequency range	DC: 0 ... 25 MHz (–3 dB) AC: 2 Hz ... 25 MHz (–3 dB)	
	Rise time	⩽ 14 ns	
	Pulse aberrations	⩽ ± 3 % (⩽ 4 % pp)	Measured at 8 div. amplitude and applied rise time of ⩾ 1 ns
	Deflection coefficients	2 mV/DIV ... 10 V/DIV	1-2-5 sequence
	Continuous control range	1 : ⩾ 2,5	uncalibrated
	Deflection accuracy	± 3 %	
	Input impedance	1 MΩ/20 pF	
	Input RC time	0.1 s	Coupling switch to AC
	Maximum permissible input voltage	400 V, d.c. + a.c. peak	
	Vertical positioning range	16 divisions	
	Dynamic range	24 divisions	
	Visible signal delay	⩾ 40 ns	
	C.M.R.R. in A-B mode	⩾ 40 dB at 1 MHz	After adjustment at d.c. or low frequencies
	Cross talk between channels	–40 dB or better at 10 MHz	
	Instability of the spot position:		
	Temperature drift	⩽ 0,3 div/hour	
1.2.2.3.	*Time base*		
	Time coefficients	0.5 s/DIV ... 0.2 μs/DIV	1-2-5 sequence
	Continuous control range	1 : ⩾ 2,5	uncalibrated
	Coefficient error	± 3 %	
	Magnification	10x	
	Magnifier error	± 2 %	

	Designation	*Specification*	*Additional information*
1.2.2.4.	*Triggering*		
	Source	External Internal Internal + External	– triggering via front panel input socket "External" – triggering via oscilloscope – triggering via analyzer – triggering via analyzer and front panel input socket "External"
	Triggering via oscilloscope	Y_A, Y_B and Composite	COMP is A and B depressed
	Triggering via analyzer	At trigger word	DATA depressed
	Triggering via analyzer + External	At trigger word and trigger qualifier	in QUAL mode (i.e. EXT and DATA depressed) and trigger qualifier is "true". "True" is at high level.
	Trigger mode	Automatic, normal AC normal DC and TV	TV line or frame switched by TIME/DIV switch. TV line : .2 µs/div ... 20 µs/div TV frame: 50 µs/div ... 5 s/div.
	Trigger sensitivity	Internal: 1.0 div. at 25 MHz or word triggering External: 0.5 Vpp at 25 MHz TV int.: 0.7 div. TV ext.: 0.35 Vpp	 Sync. pulse amplitude Sync. pulse amplitude
	Triggering frequency range	AUTO: 20 Hz ... ⩾ 25 MHz AC: 5 Hz ... ⩾ 25 MHz DC: 0 Hz ... ⩾ 25 MHz	Typically, stable triggering can still be obtained at 50 MHz and 2 div. or 1 Vpp amplitude
	Level range	AUTO: Proportional to peak-to peak value of trigger signal. AC, DC: 16 div. at internal trigg. and 8 V at external trigg.	 + or –8 div and + or –4 V referenced to centre of screen.
	Triggering slope	Positive or negative going	
	Input impedance (External socket)	1 MΩ//20 pF	
	Maximum permissible input voltage (External socket)	400 V d.c. + a.c. peak for QUAL-mode ± 50 V	
1.2.2.5.	*X Deflection*		
	Source	A, B or EXT.	As selected by trigger source switch, if TIME/DIV switch is in pos. X-DEFL.
	Deflection coefficients	A or B: as selected by switch AMPL/DIV. EXTERNAL: 0.5 V/division	
	Deflection accuracy	± 10 % in A or B	
	Frequency range	DC: 0 ... 1 MHz (–3 dB) AC: 5 Hz ... 1 MHz (–3 dB)	
	Phase shift	⩽ 3° at 100 kHz	
	Dynamic range	24 divisions	For frequencies ⩽ 100 kHz

	Designation	*Specification*	*Additional Information*
1.2.2.6.	*Calibration generator*		
	Output voltage	1.2 Vpp	Square wave
	Accuracy	± 1 %	
	Frequency	≈ 2 kHz	

1.2.3. Characteristics of the power supply

Designation	*Specification*	*Additional Information*
AC supply:	Double insulated	Safety Class II, IEC 348
Nominal voltage range (on line-mains voltage adaptor)	110, 127, 220 or 240 Va.c. ± 10 %	
Nominal frequency range	46 ... 440 Hz ± 10 %	
Power consumption	45 W max.	At nominal mains voltage
DC supply:		
Voltage range	23-27 Vd.c.	Floating input
	22-28 V	With relaxed specifications
Current consumption	1,35 A max.	
Capacity to earth	110 pF	Measured with rubber feet on earthed metal plate of 1 m^2
	23 pF	Measured 30 cm above earthed plate of 1 m^2

1.2.4. Environmental characteristics

The characteristics are valid only if the instrument is checked in accordance with the official checking procedure. Details of these procedures and failure criteria are supplied on request by the PHILIPS organisation in your country, or by N.V. PHILIPS' GLOEILAMPENFABRIEKEN, TEST AND MEASURING DEPARTMENT, EINDHOVEN, THE NETHERLANDS.

Ambient temperature		
Rated range of use	+5 °C ... +40 °C	
Limits of operation	–10 °C ... +55 °C	
Storage and transport conditions	–40 °C ... +70 °C	
Humidity	According to IEC 68 Db	
Bump	1000 bumps of 10 g, ½ sine, 6 ms duration in each of 3 directions	
Vibration	30 minutes in each of three directions, 10-150 Hz; 0.7 mm p-p and 5 g max. acceleration	
Altitude		
Limit of operation	5000 m (in open air)	is 475 mbar or 47,5 kPa
Limit of transport	15000 m (in open air)	is 100 mbar or 10,0 kPa
Recovery time	30 minutes if instrument temperature is raised from –10 °C to +20 °C at 60 % relative humidity	

Electromagnetic interference meets VDE Störgrad K.

	Designation	Specification	Additional Information
1.2.5.	**Mechanical data**		
	Dimensions:		
	Length	445 mm	Handle and controls excluded
	Width	335 mm	Handle excluded
	Height	137 mm	Feet excluded
	Weight	8 kg	

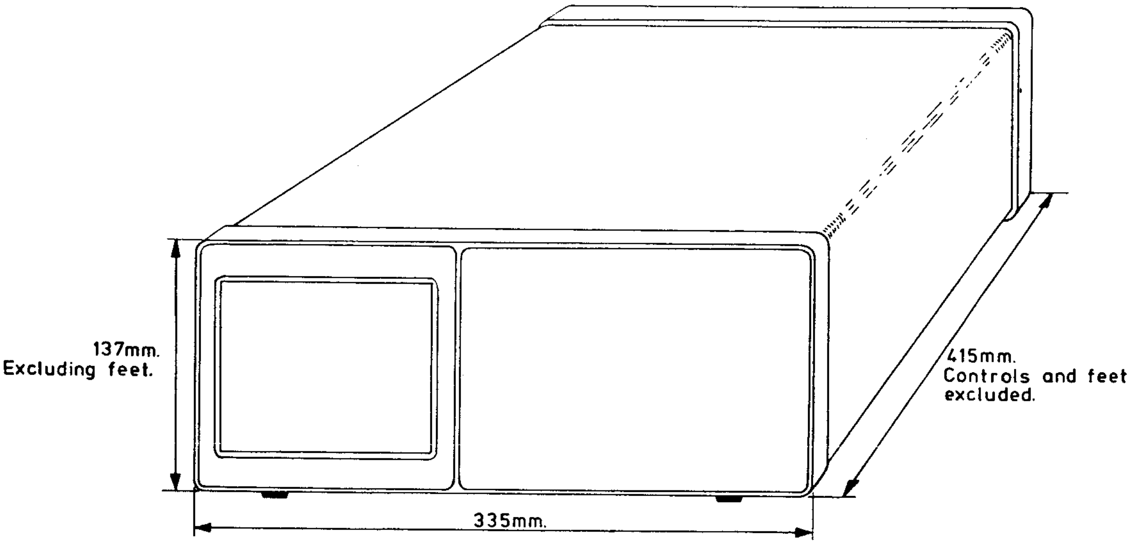

137mm.
Excluding feet.
415mm.
Controls and feet excluded.
335mm.

Fig. 1.4. Dimensions

MA9623 E

1.3. ACCESSORIES

1.3.1. Supplied with the instrument

Front cover
1 BNC 4 mm adaptor
2 Probes PM 8925
Instruction manual
3 Multi-lead probe POD's, PM 8820

1.3.2. Optional (see also section 3 "INFORMATION CONCERNING ACCESSORIES")

Analyzer probes	Multi-lead probe	PM 8820
	Extension kit	PM 8819
	Trigger qualifier extension probe	PM 8810
Oscilloscope probes	Passive probe set 1 : 1 (1,5 m) 15 MHz	PM 8921
	Passive probe set 1 : 1 (2.5 m) 15 MHz	PM 8921L
	Passive probe set 10 : 1 (1.5 m) 40 MHz	PM 8925
	Passive probe set 10 : 1 (2.5 m) 40 MHz	PM 8925L
	Passive probe set 10 : 1 (1.5 m) 75 MHz	PM 8927
	Passive probe set 10 : 1 (2.5 m) 75 MHz	PM 8927L
	HV probe set 100 : 1 (1.5 m) 5.6 kV, 150 MHz	PM 8932
	Isolation amplifier	PM 8940
	1 : 10, 10 : 1 and 100 : 1 650 MHz FET-probe	PM 8943
	Current probe PM 9355	
Sundries	Polaroid anti-glare filter	PM 8910
	Oscilloscope camera	PM 9381
	Camera adaptor PM 8972	
	19" Rack mount adaptor	PM 8963
	Collapsible viewing hood	PM 9366
	Closed long type viewing hood	PM 8980
	Rechargeable battery pack 330 V d.c./24 V d.c.	PM 8901
	Trolley PM 8991	
	Accessory pouch	PM 8992
	Banana-BNC adaptor	PM 9051
	Trimming tool kit	800/NTX

2. Directions for use

2.1. GENERAL INFORMATION

This section outlines the procedures and precautions necessary for installing the PM 3540, identifies and briefly describes the functions of the front and rear panel controls and indicators, and explains the practical aspects of operation to enable an operator to evaluate quickly the instrument's main functions.

2.1.1. **Safety regulations** (in accordance with IEC 348)

Before connecting the instrument to the mains (line), visually check the cabinet, controls and connectors, etc. to ascertain whether any damage has occured in transit. If any defects are apparent, do not connect the instrument to the mains (line).

The instrument must be disconnected from all voltage sources, and any high voltage points discharged before any maintenance or repair work is carried out. If adjustments or maintenance of the operating instrument with covers removed is inevitable, it must be carried out only by a skilled person who is aware of the hazards involved. In normal operation the double-insulated power supply obviates the need of a safety ground.
Bear in mind that the capacitors inside the instrument may still be charged even if the instrument has been separated from all voltage sources.
Never remove a circuit board until the oscilloscope has been switched off for at least one minute.
When an instrument is brought from a cold to a warm environment, condensation may cause a hazardous condition. In this situation, you must allow approximately 30 minutes (i.e. recovery time, see 1.2.4. "Environmental characteristics") for your logic-scope to acclimatize until all condensation has evaporated.

Warning: **It must be borne in mind that in all measurements the frame ground of the instrument is raised to the same potential as that of the measuring ground probe connections. Neither the probe's ground lead nor the frame ground shall be connected to live potentials.**

2.1.2. Installation, Mains adaption and connection

Before connecting the instrument to the mains (line), make sure that it is set to the local mains (line) voltage. On delivery the instrument is set to 220 V. If the instrument is to be used with 110 V, 127 V or 240 V supply, the appropriate voltage should be selected by turning the adaptor on the rear panel to indicate the voltage required (see Fig. 2.1.).

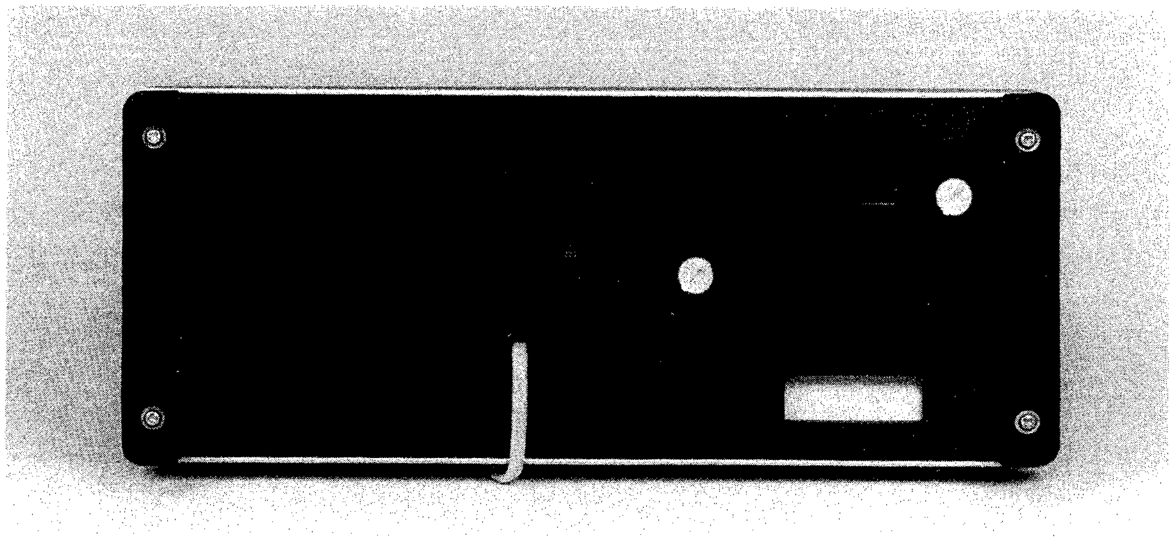


Fig. 2.1. Rear view of the logic-scope showing the voltage adapter

NOTES:

NOTES:

2.1.3.

2.1.4.

2.1.5.

2.1.6.

2.1.7.

2.1.8.

NOTES:

2.1.3. Fuse

The instrument is protected from overloads by a thermal fuse fitted between the mains (line) transformer windings. It can be replaced after having removed the instrument rear panel (see section 2.8.).
Only the fuses prescribed must be used.

2.1.4. Connection to an external supply

An external supply or battery of 23 V to 27 V capable of delivering at least 2 A can be connected to the socket on the rear panel (DC power input cord set: 4822 321 20125).

The inner conductor must be connected to the negative pole and the outer conductor to the positive pole, as indicated on the rear panel.

The instrument is protected against overloads and wrong polarity by an internal fuse and diode. This fuse can be replaced after having removed the instrument rear panel (see section 2.8.).

2.1.5. Front cover and instrument position

The front cover can be simply removed by pulling it from the front.
The instrument may be used horizontally or in several sloping positions by using the carrying handle as a tilting bracket.

2.1.6. Carrying handle

The handle can be rotated if the pushbuttons on its bearings are depressed.

2.1.7. Switching on

The POWER switch is incorporated in the graticule ILLUM control on the front panel, immediately beside the screen bezel. The associated POWER ON/OFF indicator lamp is adjacent to the ILLUM control.
The instrument must never be switched on whilst any circuit board is removed.

2.1.8. Cooling

Take care that the natural air flow through the instrument is not obstructed.
Do not position the instrument on any surface which produces or radiates heat.
Do not place any instruments or papers on top of the instrument to avoid excessive heating-up.

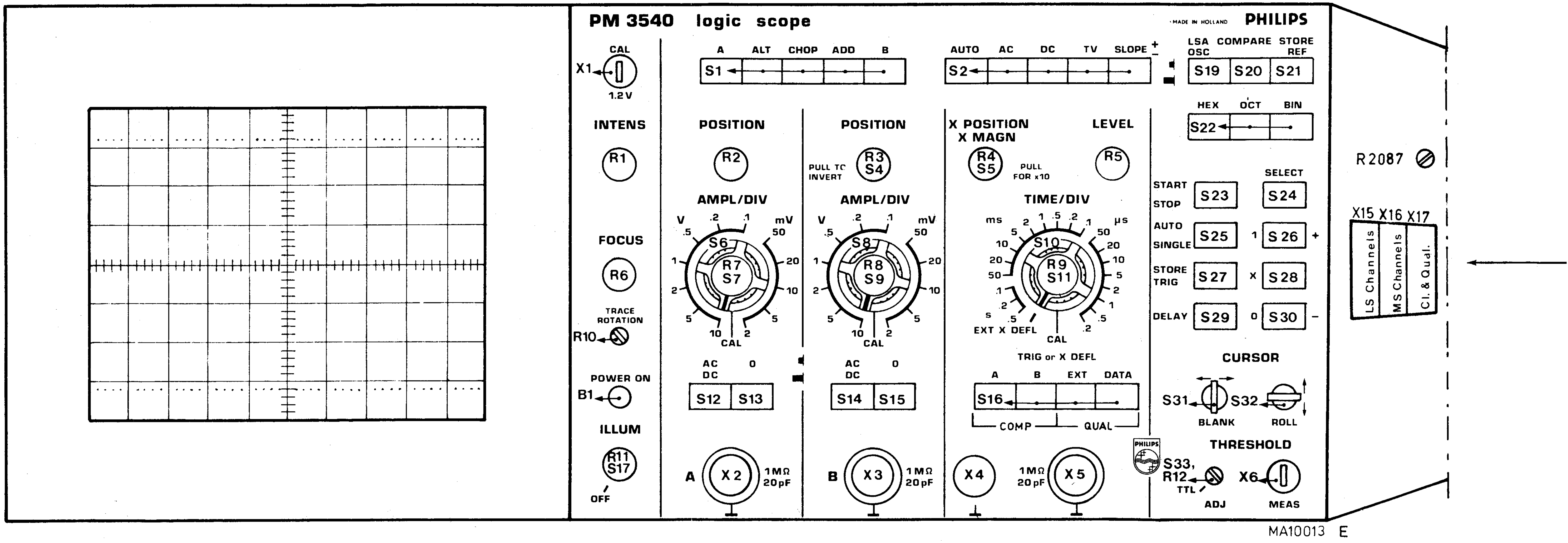
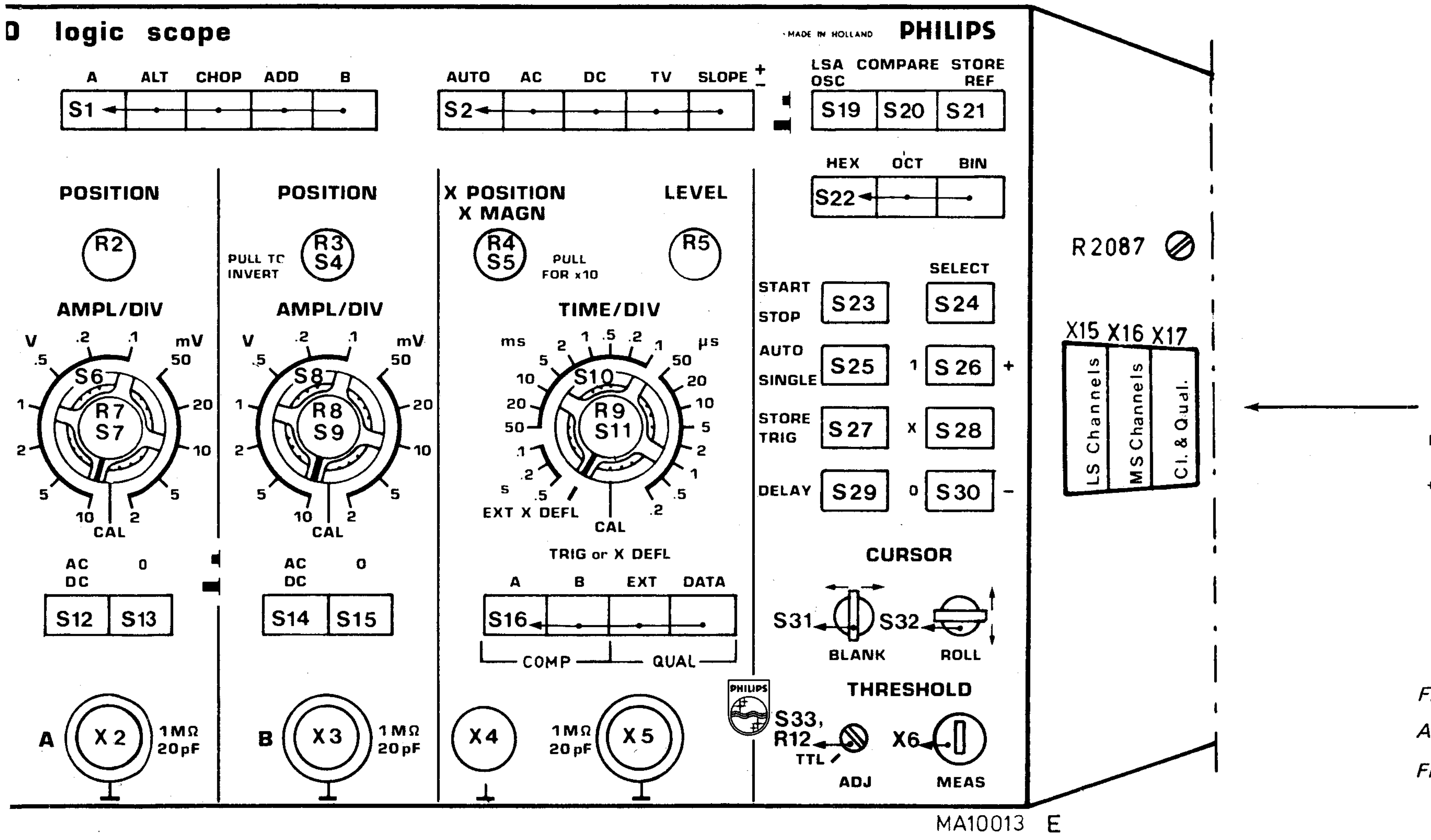

PM 3540 logic scope
MADE IN HOLLAND
PHILIPS
CAL
X1
1.2V
INTENS
R1
FOCUS
R6
TRACE ROTATION
R10
POWER ON
B1
ILLUM
R11
S17
OFF
A
ALT
CHOP
ADD
B
S1
POSITION
R2
POSITION
R3
S4
PULL TO INVERT
AMPL/DIV
V
mV
S6
R7
S7
CAL
AMPL/DIV
S8
R8
S9
AC
DC
0
S12
S13
S14
S15
A
X2
1MΩ
20pF
B
X3
1MΩ
20pF
AUTO
AC
DC
TV
SLOPE
+
−
S2
X POSITION
X MAGN
R4
S5
PULL FOR x10
LEVEL
R5
TIME/DIV
ms
μs
S10
R9
S11
EXT X DEFL
CAL
TRIG or X DEFL
A
B
EXT
DATA
S16
COMP
QUAL
X4
1MΩ
20pF
X5
LSA
OSC
COMPARE
STORE
REF
S19
S20
S21
HEX
OCT
BIN
S22
START
STOP
S23
SELECT
S24
AUTO
SINGLE
S25
1
S26
+
STORE
TRIG
S27
x
S28
DELAY
S29
0
S30
−
CURSOR
S31
S32
BLANK
ROLL
THRESHOLD
PHILIPS
S33,
R12
TTL
ADJ
X6
MEAS
R2087
X15
X16
X17
LS Channels
MS Channels
Cl. & Qual.
MA10013 E

Fig. 2.2. *Front view showing controls and sockets*

Abb. 2.2. *Frontansicht mit Bedienungselementen und Buchsen*

Fig. 2.2. *Vue avant montrant les commandes et les prises*


D logic scope
MADE IN HOLLAND
PHILIPS
A ALT CHOP ADD B
S1
AUTO AC DC TV SLOPE + −
S2
LSA OSC COMPARE STORE REF
S19 S20 S21
HEX OCT BIN
S22
POSITION
R2
POSITION
PULL TO INVERT
R3 S4
X POSITION X MAGN
R4 S5
PULL FOR x10
LEVEL
R5
AMPL/DIV
V .2 .1 mV .5 50 1 20 2 10 5 5 10 2
S6 R7 S7
CAL
AMPL/DIV
S8 R8 S9
CAL
TIME/DIV
ms 2 1 .5 .2 .1 μs 5 50 10 20 20 10 50 5 .1 2 .2 1 s .5 .5 .2
S10 R9 S11
EXT X DEFL
CAL
START STOP
S23
SELECT
S24
AUTO SINGLE
S25
1 S26 +
STORE TRIG
S27
x S28
DELAY
S29
0 S30 −
CURSOR
S31 S32
BLANK ROLL
AC DC 0
S12 S13
AC DC 0
S14 S15
TRIG or X DEFL
A B EXT DATA
S16
COMP QUAL
THRESHOLD
S33, R12
TTL ADJ
X6 MEAS
A X2 1MΩ 20pF
B X3 1MΩ 20pF
X4
1MΩ 20pF X5
R2087
X15 X16 X17
LS Channels
MS Channels
Cl. & Qual.
MA10013 E

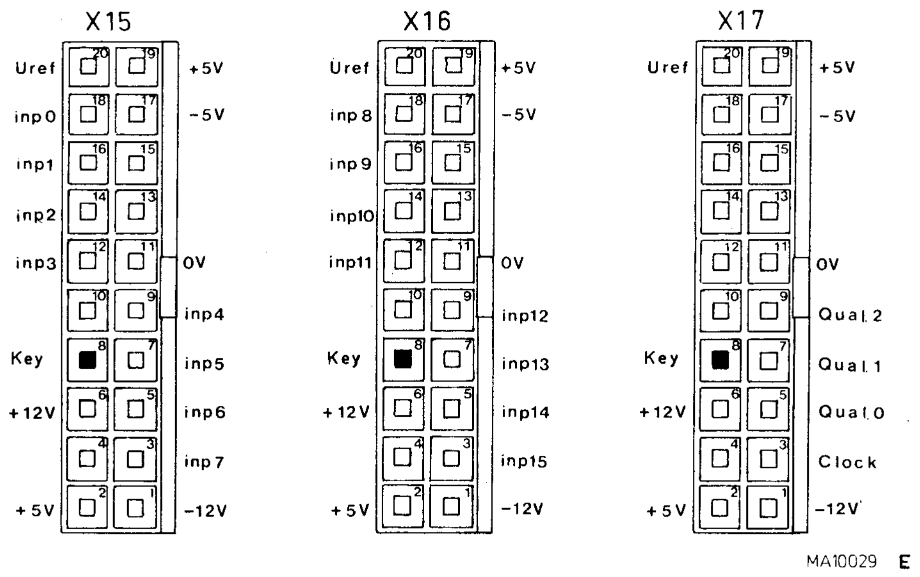

X15
Uref 20 19 +5V
inp0 18 17 −5V
inp1 16 15
inp2 14 13
inp3 12 11 0V
10 9 inp4
Key 8 7 inp5
+12V 6 5 inp6
4 3 inp7
+5V 2 1 −12V
X16
Uref +5V
inp8 −5V
inp9
inp10
inp11 0V
inp12
Key inp13
+12V inp14
inp15
+5V −12V
X17
Uref +5V
−5V
0V
Qual.2
Key Qual.1
+12V Qual.0
Clock
+5V −12V
MA10029 E

Fig. 2.2.1. Data input sockets (front view)

Abb. 2.2.1. Dateneingangsbuchsen für Analysator

Fig. 2.2.1. Prises pour l'entrée des données

2.2. CONTROLS AND SOCKETS (refer to Fig. 2.2.)

2.2.1. Controls and sockets of the analyzer part

2.2.1.1. Mode

Function selection switch	2-way pushbutton switch
LSA (depressed)	Analyzer mode is selected
OSC (released)	Oscilloscope mode is selected.
COMPARE pushbutton	The captured data block is compared with the reference data block.
STORE REF pushbutton	Data is transferred from input memory into reference memory. (If COMPARE knob is depressed.)

2.2.1.2. Display

HEX pushbutton	Selecting the state table in hexadecimal format
OCT pushbutton	Selecting the state table in octal format
BIN pushbutton	Selecting the state table in binary format.
BLANK tumbler switch S31 (pushbutton SELECT released)	"Right" position: data presentation channels (columns) are blanked starting at channel 15 as long as this position is activated.
	"Left" position: blanked channels (columns) are displayed again in reversed direction as "Right" position.
CURSOR tumbler switch S31 (pushbutton SELECT depressed) Cursor is an intensified digit in the heading of the display	This mode provides cursor shift for parameter selection. "Right" position: direction of the cursor is to the right "Left" position: direction of the cursor is to the left.
ROLL tumbler switch S32 (pushbutton SELECT released)	"Upper" position: displayed format rolls upwards through the 64 words memory
	"Lower" position: displayed format rolls downwards through the 64 words memory.
CURSOR tumbler switch S32 (pushbutton SELECT depressed) Cursor is an intensified digit in the heading of the display.	This mode provides cursor shift for parameter selection. "Upper" position: the cursor moves upwards "Lower" position: the cursor moves downwards.
SELECT pushbutton (parameter selection)	To specify the clock edge, clock qualifiers, trigger word and delay. The status of the parameters are given in the heading of the display.
Selection pushbuttons	Setting the parameters.
"1" function	"1" pushbutton selects "true" for a high level or positive going clockedge.
"0" function	"0" pushbutton selects "true" for a low level or negative going clockedge.
"X" function	"X" pushbutton selects don't care.
"+" function	Add function: $0 \ldots 9_{DEC.}$, $0 \ldots F_{HEX.}$ and $0 \ldots 7_{OCT.}$
"–" function	Subtract function: $9 \ldots 0_{DEC.}$, $F \ldots 0_{HEX.}$ and $7 \ldots 0_{OCT.}$
DELAY pushbutton	Activates the trigger delay. Pushbuttons "+" and "–" set the value of the trigger delay. "+" counts up. "–" counts down.
STORE TRIG pushbutton	After depressing this pushbutton, the contents of the top row (i.e. the 1st word) of the displayed format becomes automatically the new trigger word, including the blanked channels or columns (instrument **not** in the COMPARE mode).

2.2.1.3. *START*

START/STOP pushbutton	Single position pushbutton with two functions: – first push operation starts data acquisition – second push operation stops data acquisition
Acquisition mode switch	2-way pushbutton switch.
SINGLE (released)	Data is captured in a single sample
AUTO (depressed)	Data is captured in automatically repeated samples.

2.2.1.4. *THRESHOLD*

ADJ/TTL (R12/S33)	Screwdriver adjustment for variable threshold. Variable from 0 V up to +10 V. TTL threshold voltage of +1,4 V, fixed.
MEAS.	Output socket supplying the fixed +1.4 V TTL voltage or the adjusted threshold voltage.

2.2.1.5. *Miscellaneous*

Y-POSITION (R2087) Screwdriver adjustment	Continuously variable control giving vertical shift of the display in the analyzer mode.
Input X5 ("EXTERNAL")	BNC socket, input for trigger qualifier or trigger signal. See also section 2.2.2.4.
Input X15	Multi-lead connector to provide input for the 8 least significant channels.
Input X16	Multi-lead connector to provide input for the 8 most significant channels.
Input X17	Multi-lead connector to provide input for the clock and the clock qualifier signal.

2.2.2. **Controls and sockets of the oscilloscope part**

(Including the combined analyzer/oscilloscope functions)

2.2.2.1. *Mode*

Function selection switch	2-way pushbutton switch
OSC (released)	Oscilloscope mode is selected
LSA (depressed)	Analyzer mode is selected.

2.2.2.2. *Vertical channels*

Display mode switch	Function 5-way pushbutton switch selecting the vertical display mode. With all buttons released, the ALT mode is in operation.
A	Vertical deflection is achieved by the signal connected to input of channel A.
ALT	The display is switched over from one vertical channel to the other at the end of every cycle of the time-base signal.
CHOP	The display is switched over from one vertical channel to the other at a fixed frequency (f ≈ 500 kHz).
ADD	Vertical deflection is achieved by the sum signal of channels A and B (or –B).
B	Vertical deflection is achieved by the signal connected to the input of channel B.

POSITION	Continuously variable controls giving vertical shift of the display.
PULL TO INVERT B	Push-pull switch combined with the channel B POSITION control. When pulled, channel B signal is inverted.
AMPL/DIV (outer knob)	Step control of the vertical deflection coefficients, ranging from 2 mV/div up to 10 V/div in a 1-2-5 sequence.
AMPL/DIV (centre-knob)	Continuously variable control of the vertical deflection coefficients. Note that the deflection coefficient is calibrated only with the centre-knob switched to the CAL position (fully-clockwise).
Input coupling switch	Signal coupling; 2-way pushbutton switch.
AC (depressed)	Coupling via a blocking capacitor
DC (released)	Direct coupling
0 (depressed)	Connection between input circuit and input socket is interrupted and the input circuit is grounded.
Y_A	BNC socket for channel A input
Y_B	BNC socket for channel B input

2.2.2.3. *Triggering*

Trigger mode switch	Function
	5-way pushbutton switch, selecting the trigger mode and the polarity of the trigger transition. With all pushbuttons released AUTO sweep mode is in operation at a fixed range of the LEVEL control.
AUTO	A trace is displayed in the absence of trigger signals. The range of the LEVEL control is proportional to the peak-to-peak value of the triggering signal.
AC	Normal triggering and fixed range of the LEVEL control. DC component of trigger signal is blocked.
DC	Normal triggering and fixed range of the LEVEL control. DC component of trigger signal is passed.
TV	Line or frame synchronisation is obtained as dicated by TIME/DIV switch (frame from .5 s/div to 50 μs/div and line from 20 μs/div to .2 μs/div).
+/–	Sweeps are triggered on positive or negative-going trigger signal transitions. In TV, – must be selected for negative video signals and + for positive video signals.
LEVEL	Control for continuously varying the level of the waveform on which the display is to start.
TRIG OR X DEFL	See TRIG or X DEFL source switch in section 2.2.2.4. below.

2.2.2.4. *Horizontal channel*

TRIG or X DEFL source switch	Function
	4-way pushbutton switch selects the trigger source or the source of horizontal deflection if the TIME/DIV switch is the X DEFL position. With all pushbutton released source A is selected.
A	Signal derived from channel A.
B	Signal derived from channel B.

COMP (A & B both depressed; inoperative with X DEFL)	Signal derived after the electronic channel switch. Triggering occurs on the waveforms as presented on screen.
EXT	Triggering or X-deflection on signal derived from a voltage applied to the input socket X5 ("EXTERNAL").
DATA	Internal triggering on signal derived from captured data when trigger-word is recognized.
QUAL (EXT & DATA both depressed)	Internal triggering on signal derived from captured data when trigger-word is recognized, conditioned with a trigger qualifier signal applied to the input socket X5 ("EXTERNAL").
X POSITION X MAGN	Continuously variable control giving horizontal shift of the display; incorporates a push-pull switch which increases the horizontal deflection by a factor of 10 (only in the OSC mode).
TIME/DIV (outer part)	Selects the time coefficient from .2 µs/div to .5 s/div in a 1-2-5 sequence Dictates line or frame triggering in TV mode. In position X DEFL horizontal deflection is determined by TRIG or X DEFL switch.
TIME/DIV (centre knob)	Continuously variable control of the time coefficients. Must be in CAL position (i.e. fully clockwise) for the time axis to be calibrated according to the indication of the TIME/DIV switch.
Input X5 ("EXTERNAL")	BNC socket: Input for external trigger or horizontal deflection signal. Input for trigger amplifier signal.

2.2.2.5. *Miscellaneous*

CAL	Output socket supplying a squarewave of $\approx$ 2 kHz and an amplitude of 1.2. $V_{p\text{-}p} \pm$ 1 %. To be used for probe compensation and/or checking vertical deflection accuracy.
External supply	Input socket at the rear of the instrument allows the instrument to be operated by an external d.c. supply. Rated supply voltage 23 V to 27 V, current capability $>$ 2 A.
LINE (MAINS) VOLTAGE ADAPTOR	Must be set according to section 2.1.2. before the instrument is connected to the local mains voltage.

2.2.3. Cathode-ray tube and POWER controls

ILLUM POWER ON	Continuously variable control of the graticule illumination; incorporates mains (line) switch. Pilot lamp indicates the ON state.
INTENS	Continuously variable control of the trace brilliance.
FOCUS	Allows beam to be focussed for minimum spot size.
TRACE ROTATION	Screwdriver adjustment to align the trace with the horizontal graticule lines.

2.3. OPERATING INSTRUCTIONS

2.3.1. Switching on the instrument

Before connecting the instrument to any supply, the instructions given in section 2.1. Installation, should be carefully carried out.
The instrument will meet specifications (see section 1.2.) normally after a warming-up period of approximately 15 minutes. However, if the instrument has been subjected to an extremely cold environment (e.g. left in a car overnight in freezing conditions) and is then brought in for use in a warm room, a warming-up period of sufficient length should be allowed (see 1.2.4.).

2.3.2. Preliminary procedure

This procedure is a general indication of whether the instrument is functioning correctly and provides a suitable starting point before any measurement are made.
Refer to Fig. 2.2. for location of controls.
Set INTENS and FOCUS controls in mid position.
Depress both "0" pushbuttons.
Depress AUTO and select an average time coefficient between 10 μs/div and 10 ms/div with the TIME/DIV switch. With all other pushbuttons normal (not depressed) channel A and channel B traces can be positioned on the screen with the relevant POSITION controls. Set the INTENS control for a display of medium brightness and adjust FOCUS control for well focussed traces.

2.3.3. Power-on test

When switching-on, the microprocessor initiates a test program to check the immediate microprocessor environment.
If this test gives a faulty result the c.r.t. of the instrument remains blank.
If only RAM is faulty, the wrong address is displayed binary.

2.3.4. Service test

The instrument is provided with a test program as an aid to pin-point any functional defect.
This program is selected by pressing STORE TRIG and STORE REF pushbuttons simultaneously.
The test program consists of a number of separate test modules, sequentially activated.
The first module is entered when selecting the test program.
A testmodule is dealing with a particular way of testing or with the testing of a particular part of the circuit.
To go to the next testmodule the START/STOP button has to be pressed and released.
Pressing the STORE REF and the 0 pushbuttons simultaneously leads to a return back to the operational program.
More information about the "service test" will be given in the SERVICE MANUAL of this instrument.

2.4. LOGIC STATE ANALYZER MODE

With the PM 3540 in this mode, the user can examine the software instructions given in the same way as they were designed. For example:

- displays can be made in binary, octal or hexadecimal to suit the individual application.
- the display of 16 serial bits x up to 16 parallel channels (i.e. display window) can be paged through the captured data block of 64x16 bits.
- the captured data block can be shifted easily up- and downstream relative to a pre-selected word (trigger-word) in the data stream.
- a reference block of data can be compared with a second block of captured data, in order to quickly and conveniently locate a fault.
- the instrument can then be set to trigger on the fault or in the vicinity of the fault.

With all these facilities, the user can make a detailed and meaningful analysis of any digital problem.

2.4.1. Data acquisition

Data acquisition is the process by which digital signals are sampled and converted into binary form.
For conversion into binary form, see "THRESHOLD" section (2.4.2.).
The data which has to be displayed must be applied to the right side panel inputs (X15, X16 and X17) via the appropriate PM 8820 probe Pod's (for characteristics concerning this probe Pod, see Chapter 3.). Note that unused inputs of the probe automatically result in zero level signals (refer also the "Channel blanking" section 2.5.4.).

2.4.2. Threshold level

To achieve proper data acquisition, the logical binary state of the incoming data, has to be converted into proper binary pulses.
To do this, the threshold voltage must be set correctly.
This is automatically done for the TTL level; also a variable threshold (ADJ.) has been built-in.
To set the threshold value in the ADJ mode, connect a voltmeter to the output socket MEAS and adjust the corresponding potentiometer (screwdriver adjustment).
Note that the threshold value only applies if the PM 8820 probes are used and that the threshold value can not be selected for inputs X15 (least sign. channels), X16 (most sign. channels) and X17 (clock & qualifiers) separately.
Correct earth connection of each probe POD is strongly recommended.

2.4.3. Clock

The clock is a repetitive signal, which determines the frequency of samples taken from the applied measuring signals. At each clock pulse, a sample of the applied signals is taken and stored in the input memory of the PM 3540.
The above action is started by the START function and stopped by the STOP function of the START/STOP pushbutton, or automatically by depressing the AUTO/SINGLE pushbutton.

As clock signal is taken a signal derived from the system clock (or other signal) present in the instrument which must be tested. This is called a synchronous clock, because the analyzer's sample actions are running in synchronization with the system under test. The clock action can be selected at the positive or negative going edge of the system clock.

2.4.4. Clock qualifier

The clock qualifier allows more selective data acquisition by gating the clock with an additional condition which can be "1", "0" or "X" (don't care), selectable with the selection pushbuttons 1, 0 or X.

2.4.5. Triggering (see Chapter 1.2. for characteristics)

The trigger action stops data acquisition and storage, the input memory holds the data stored before the trigger was received.
The memory content is available to be displayed (point 2.4.5. is valid without TRIGGER DELAY).

Trigger source can be chosen from:
- a certain selected word occuring in the input data stream (i.e. internal triggering)
- an externally applied signal
- manual.

2.4.5.1. *Internal triggering*

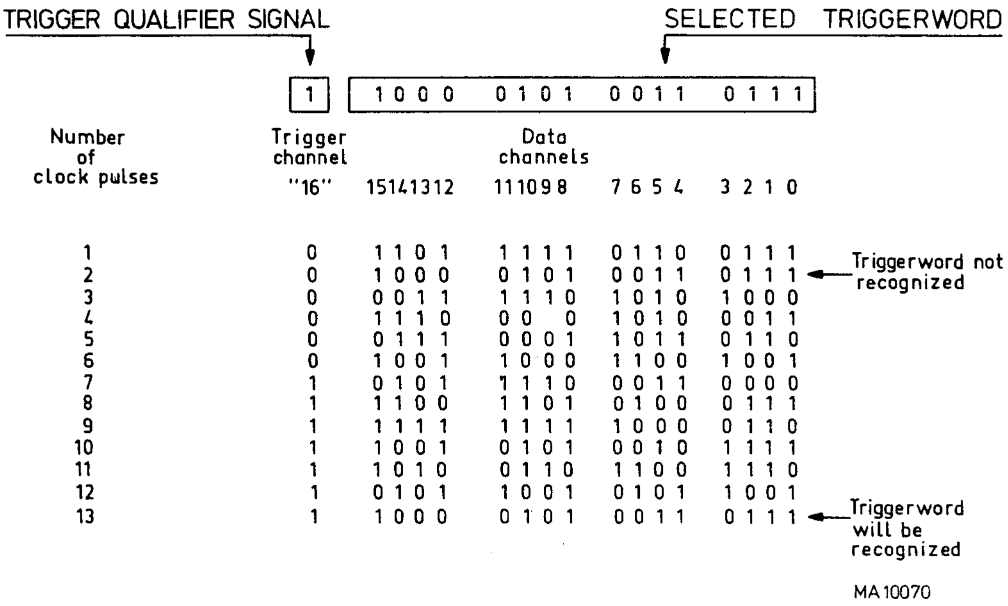
Triggering takes place when the analyzer recognises a match between a word in the data stream and a certain pre-selected trigger word.
This trigger word consists of a combination of logic "1" and "0" 's, which can be selected by means of the SELECTION pushbuttons (see 2.5.2.) or from the display with the aid of the pushbutton "STORE TRIG".
Input channels which are not used, or of which the bit information is not important, the X-function (don't care) has to be selected.
Internal triggering can be combined with trigger delay and trigger qualifier.

2.4.5.2. *External triggering*

Triggering takes place by an external signal, applied to the front panel BNC socket "EXTERNAL". Triggering only occurs, when the trigger input is "true" at the clock edge and the triggerword consists of don't cares (X ... X).
External triggering is effective in the "QUAL" mode and can be combined with trigger delay.

2.4.5.3. *Manual triggering*

Triggering takes place by pushing the START/STOP button when the message "NOT TRIGGERED" has been displayed; this overrules all other trigger conditions (the trigger delay as well). Manual triggering is useful to display captured data, even if the triggerword is unknown or unfindable.



Number of clock pulses	Trigger channel	Data channels			
	"16"	15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
1	0	1 1 0 1	1 1 1 1	0 1 1 0	0 1 1 1
2	0	1 0 0 0	0 1 0 1	0 0 1 1	0 1 1 1
3	0	0 0 1 1	1 1 1 0	1 0 1 0	1 0 0 0
4	0	1 1 1 0	0 0 0	1 0 1 0	0 0 1 1
5	0	0 1 1 1	0 0 0 1	1 0 1 1	0 1 1 0
6	0	1 0 0 1	1 0 0 0	1 1 0 0	1 0 0 1
7	1	0 1 0 1	1 1 1 0	0 0 1 1	0 0 0 0
8	1	1 1 0 0	1 1 0 1	0 1 0 0	0 1 1 1
9	1	1 1 1 1	1 1 1 1	1 0 0 0	0 1 1 0
10	1	1 0 0 1	0 1 0 1	0 0 1 0	1 1 1 1
11	1	1 0 1 0	0 1 1 0	1 1 0 0	1 1 1 0
12	1	0 1 0 1	1 0 0 1	0 1 0 1	1 0 0 1
13	1	1 0 0 0	0 1 0 1	0 0 1 1	0 1 1 1

Fig. 2.3. Triggerword plus trigger qualifier

2.4.6. **Trigger qualifier**

The trigger qualifier is provided as an extra conditional signal for the selected internal triggerword. The trigger qualifier signal is input via the front panel BNC socket "EXTERNAL" and is effective in the "QUAL" mode.

The trigger qualifier allows more selective data acquisition by gating the trigger signal with an additional condition which can be seen as a 17th channel for trigger recognition (see Fig. 2.3.).
This input is "true" at high level (for characteristics see 1.2.1.5.).
Connecting the trigger qualifier extension probe PM 8810 to this input, the trigger selection capacity can be extended.

2.4.7. Trigger delay

By pushing the "DELAY" button the trigger delay is switched on. The trigger delay is a number of clock pulses, elapsing between appearance of the trigger word or external trigger signal, and the actual moment of triggering. This means that the data block to be measured can be positioned downwards in the data stream (see Fig. 2.4.).

Post triggering

Using the trigger delay, virtually any data block downstream from the initial triggerword (or trigger signal) can be selected.
The trigger delay value can be selected between 1 and 999 system clock pulses and is shown in the heading of the display. When for example the trigger delay is set to 63, the complete memory content is refreshed with data which appeared just after the trigger-word (or trigger signal), see Fig. 2.4.).

Pre-triggering

If the trigger delay is switched-off (reset the "DELAY" button) or the trigger delay has been set to 0, triggering takes place, at the same moment that the triggerword is present on the data inputs. In this case the memory contains, 63 data words, which are captured just before the trigger word (or trigger signal) see Fig. 2.4.
This mode is indicated by a minus character in the display.

Centre triggering

This is, when the triggerword is brought into the centre of the captured data block.
For this, a trigger delay of 32 clock pulses has to be selected (see Fig. 2.5.).

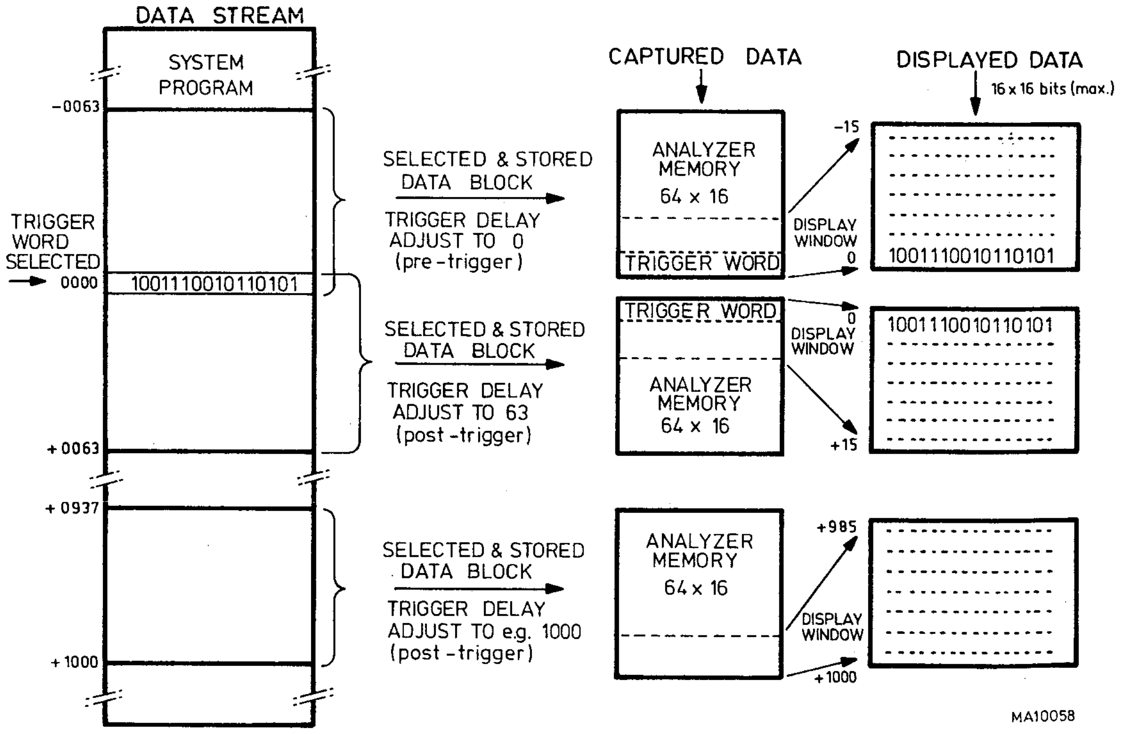

DATA STREAM
SYSTEM PROGRAM
-0063
TRIGGER WORD SELECTED
0000
1001110010110101
+0063
+0937
+1000
SELECTED & STORED DATA BLOCK
TRIGGER DELAY ADJUST TO 0 (pre-trigger)
SELECTED & STORED DATA BLOCK
TRIGGER DELAY ADJUST TO 63 (post-trigger)
SELECTED & STORED DATA BLOCK
TRIGGER DELAY ADJUST TO e.g. 1000 (post-trigger)
CAPTURED DATA
ANALYZER MEMORY 64 x 16
TRIGGER WORD
DISPLAYED DATA
16 x 16 bits (max.)
-15
0
+15
+985
+1000
DISPLAY WINDOW
1001110010110101
MA10058

Fig. 2.4. Relationship between trigger delay, memory and display

2.4.8. **Display** (see Fig. 2.5.)

In the analyzer mode the display exhibits data on the oscilloscope CRT in a truth table-type format.
The data can be shown in binary, octal or hexadecimal form.
The continuously displayed heading in the top part of the screen contains information about the parameters and the status of the instrument.
Line indications are memory locations related to the captured triggerword so that the position of the displayed detail (i.e. display window) is known at all times.

2.4.8.1. Paging

As illustrated in Fig. 2.5. the actual display on the screen is a 16 word data block (i.e. display window) within the total captured data block.
In order to display the rest of the captured data the "roll" facility of the cursor control is used, which allows the user to page through the entire 64 word data block.

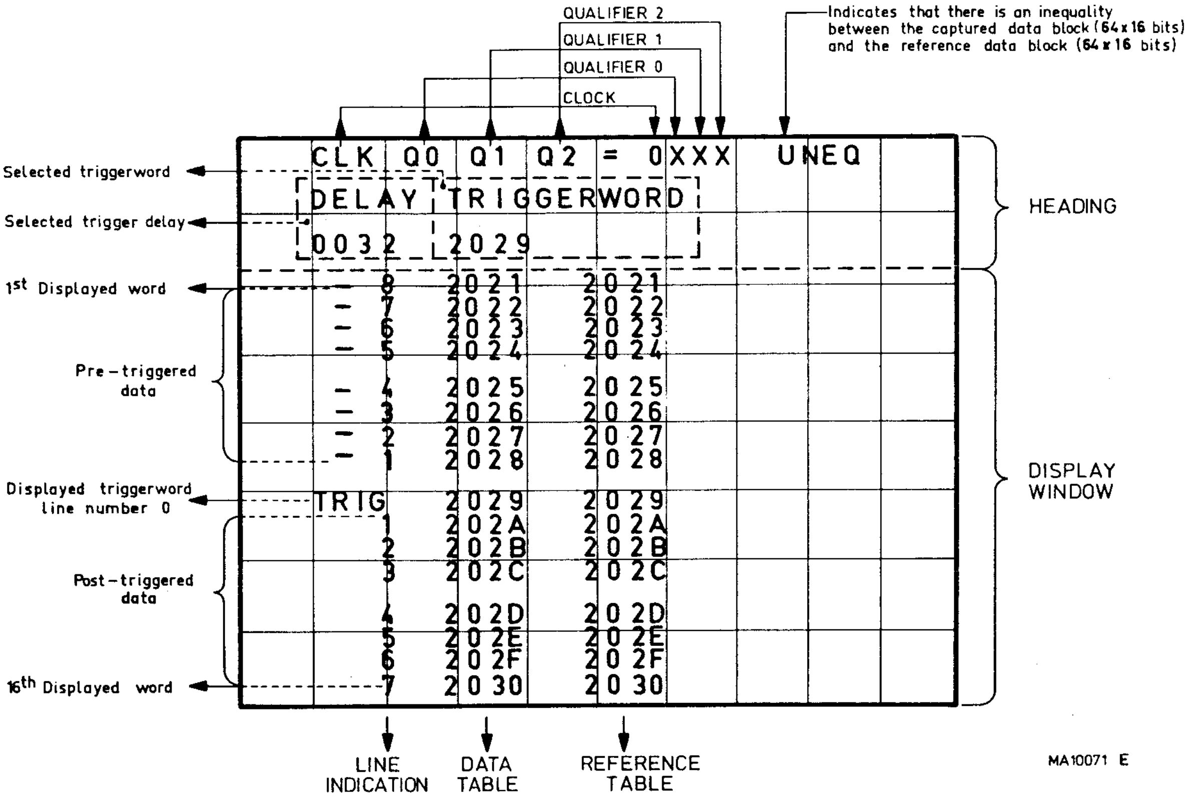

QUALIFIER 2
QUALIFIER 1
QUALIFIER 0
CLOCK
Indicates that there is an inequality between the captured data block (64x16 bits) and the reference data block (64x16 bits)
CLK Q0 Q1 Q2 = 0XXX UNEQ
DELAY TRIGGERWORD
0032 2029
- 8 2021 2021
- 7 2022 2022
- 6 2023 2023
- 5 2024 2024
- 4 2025 2025
- 3 2026 2026
- 2 2027 2027
- 1 2028 2028
TRIG 2029 2029
1 202A 202A
2 202B 202B
3 202C 202C
4 202D 202D
5 202E 202E
6 202F 202F
7 2030 2030
Selected triggerword
Selected trigger delay
1st Displayed word
Pre-triggered data
Displayed triggerword line number 0
Post-triggered data
16th Displayed word
HEADING
DISPLAY WINDOW
LINE INDICATION
DATA TABLE
REFERENCE TABLE
MA10071 E

Fig. 2.5. Display

2.5. SELECTION OF THE LOGIC STATE ANALYZER MODE

By depressing pushbutton LSA/OSC the analyzer mode is selected and the input signals which have to be displayed are simultaneously clocked into an input memory at a sample clock transition with respect to the selected threshold level.
The format of the input memory is 64x16 bit words.

2.5.1. Parameter selection mode

With pushbutton SELECT depressed the instrument is in the selection mode.
Before logic analysis can be made, the triggerword, clock edge, clock qualifiers and possible trigger delay must be selected. To do this the parameters can be specified by use of the horizontal cursor control, the vertical cursor control and the selection pushbuttons 1/+, X (don't care) and 0/–,
These selection pushbuttons can be used step by step or continuously.
With pushbutton SELECT, in the released position, data input can be started by pushing the START-button or depressing the AUTO-button.

2.5.2. Selection pushbuttons

The selection buttons enable the user to specify the parameters in the heading and represent different functions dependable on the various parameters and the display mode.

"1, +" : Pushbutton with automatic release.

function "1" : logical one for – trigger word in BIN format
– qualifier and clock

function "+" : add function for – delay in 0-9 cycle
– trigger word in the case of: HEX format in 0-F cycle
OCT format in 0-7 cycle

"X" : Pushbutton with automatic release.

function "X" : don't care for – trigger word in BIN format
– qualifier and clock

"0, –" : Pushbutton with automatic release.

function "0" : logical zero for – trigger word in BIN format
– qualifier

function "–" : subtract function for – delay in 9-0 cycle
– trigger word in the case of: HEX format in F-0 cycle
OCT format in 7-0 cycle.

2.5.3. Cursor and CURSOR controls

In the select mode (i.e. pushbutton SELECT depressed) the cursor is identified by an intensified digit in the heading of the display and is positioned by the cursor controls in horizontal or in vertical direction.

2.5.4. ROLL and BLANK controls

When the instrument is **not** in the select mode (i.e. pushbutton SELECT released), the vertical cursor control is used as a roll function to provide paging through the entire 64-word memory.

The horizontal cursor control is used to blank channels.
In the Table modes blanking results in suppression columns from the left (i.e. channel 15) to the right (i.e. channel 0), see Fig. 2.6.
Recalling occurs by operating the horizontal cursor control in the reverse direction.

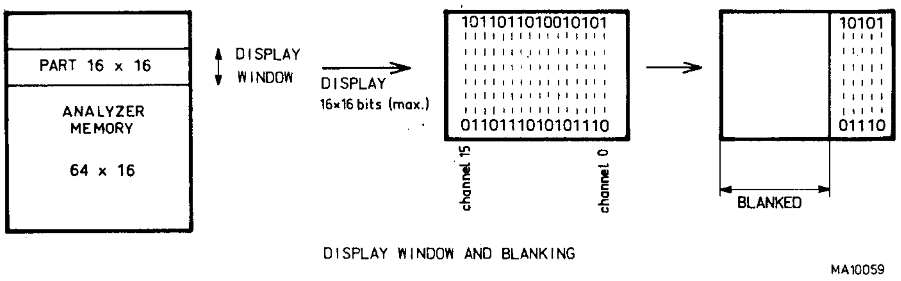


Fig. 2.6. Display window and blanking

2.5.5. Triggerword selection

After depressing the SELECT pushbutton the cursor appears in the heading of the display. The position then has to be adjusted to the triggerword position by using the horizontal or the vertical cursor control. When a triggerword is displayed in binary, the cursor can be positioned on one of the 16 digits and a "1", "0" or "X" (don't care) logic state is selected via pushbuttons 1/+, X and 0/–.
The cursor moves automatically to the next digit position. In octal or hexadecimal the horizontal cursor switch has to be used after selection via pushbuttons 1/+, X or 0/–.
The "+" pushbutton is used to reach the required 0 ... 7 or 0 ... F position. With the "–" pushbutton the sequence is 7 ... 0 or F ... 0.

2.5.6. Clock edge and Clock qualifier selection

After the SELECT pushbutton is depressed and the cursor is brought to the most top-left position of the screen the leading edge "1" or the trailing edge "0" can be selected via pushbuttons 1/+ and 0/–.
The next 3 positions are used for qualifying data acquisition. This means that data is only acquired when up to three additional logic conditions are fulfilled.
This can be done by selecting "1", "0" or "X" conditions, for the three qualifier inputs.

Note: If a clock qualifier is not connected, zero level is supplied.

2.5.7. START/STOP pushbutton

This is a one position control with two push functions:

- First push operation is the start function.
  This function initiates the moment at which the analyzer starts data capturing and recording.
- Second push operation stops capturing data .

The START/STOP control can be operated in AUTOmatic and SINGLE mode (see Fig. 2.7. and 2.8.).

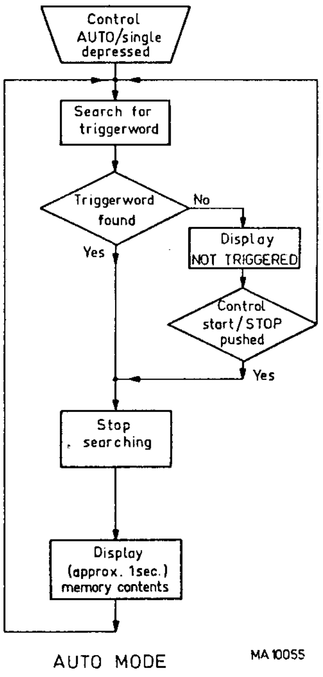

Control
AUTO/single
depressed
Search for
triggerword
Triggerword
found
No
Yes
Display
NOT TRIGGERED
Control
start/STOP
pushed
No
Yes
Stop
searching
Display
(approx. 1sec.)
memory contents
AUTO MODE
MA 10055

Fig. 2.7. Start/Stop operation in Auto mode

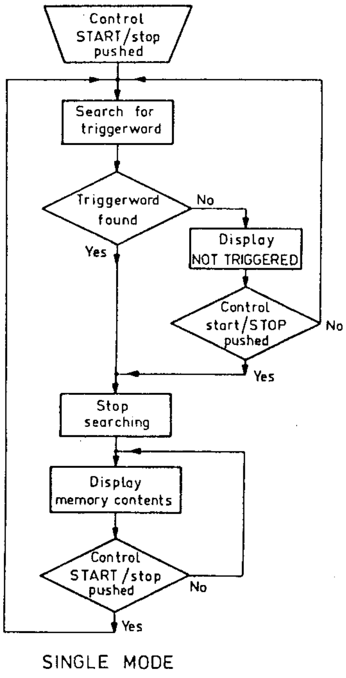

Control
START/stop
pushed
Search for
triggerword
Triggerword
found
No
Yes
Display
NOT TRIGGERED
Control
start/STOP
pushed
No
Yes
Stop
searching
Display
memory contents
Control
START/stop
pushed
No
Yes
SINGLE MODE

Fig. 2.8. Start/stop operation Single mode

2.5.8. AUTO/SINGLE mode

Data can be captured in two ways:

- AUTOmatically repeated sampling
- SINGLE sampling via manual START

In the AUTO mode (control depressed) sampling data occurs every second, which results in a continuous "refreshing" of the (input) memory contents and thus the displayed truth tables.
Automatic sampling is stopped when the AUTO/SINGLE control is set to the SINGLE position (see flow chart Fig. 2.7., START/STOP operation in the AUTO mode).

This mode is used when monitoring repetitive sequences, because individual bit changes can be detected easily.

In the SINGLE mode (control released) data input starts at a START operation and stops when the selected triggerword matches a data word in the data stream or after a STOP operation (see flow chart Fig. 2.8., START/STOP operation in the SINGLE mode). This means that the (input) memory is filled with data captured in one single sweep. The SINGLE mode provides a continuously displayed "snap shot" of the contents of the (input) memory. This feature is used to analyze a specific part of the data stream.

2.5.9. STORE TRIGgerword pushbutton

The STORE TRIG pushbutton is a single position control which is effective after pressing (but **not** in the COMPARE mode). When the STORE TRIG control is pressed, the 1st displayed word of the display window (including the present value of the blanked channels) becomes the "new" selected trigger word and will also be displayed in the heading (see Fig. 2.5.).

The store facility for a "new" triggerword can be used to represent a fault condition.

For example, a fault condition in the data stream is displayed. This fault condition is shifted to the 1st word position by means of the ROLL control, after which it is stored as a "new" triggerword. The instrument then will trigger only when this particular fault occurs.

2.5.9.1. STORE TRIG in the AUTO mode

This mode is selected when the pushbuttons AUTO and STORE TRIG are depressed.

With this facility, paging can be extended beyond the captured data block. This means that after each STORE TRIG operation a new triggerword is selected and thus automatically a new data block with new information.

This mode can also be combined with trigger DELAY.

2.5.10. TRIGGER DELAY selection

After depressing the SELECT and DELAY pushbuttons and the cursor is brought to the delay position the delay parameter can be selected. The cursor has to be positioned on each of the four digit positions, which are then set in a 0 ... 9 cycle using the "+" pushbutton or 9 ... 0 with the "–" pushbutton.

The trigger can be delayed by 1 ... 9999 clock pulses.

Trigger delay is switched off by re-pressing pushbutton DELAY.

2.5.11. COMPARE mode selection

With the pushbutton COMPARE depressed, a new recording is compared with a previously stored good recording (see section 2.5.12. "Store reference"). A second 64 word memory is used to store reference data.

The captured data block of 64 words is compared with the reference data block.

Any inequality between the two blocks is indicated in the heading of the display by the message "UNEQ" and in the display format by intensified digits. In the HEX and OCT mode both the input and reference tables are displayed. In the BIN mode, only the data input table is shown. All bits in error are intensified e.g. an intensified 0 should be a 1 or vice versa.

Note: The appearance of "EQ" or "UNEQ" in the heading of the display, indicates whether the last array of 16x64 bits captured was or was not equal to the previously stored display.

2.5.11.1. COMPARE in the AUTO mode

This mode is selected when the pushbuttons COMPARE and AUTO are depressed.

Data is input and compared automatically.

This mode is very useful for data which might differ only incidentally.

As soon as any difference between the captured data and the reference data is detected data acquisition is stopped.

The inequality is indicated by the message "UNEQ" in the heading of the display and by a flashed character in the display.

If the inequality is not displayed, it can be brought on the screen with the aid of the ROLL control.

Data input can be restarted by pushing the START-button.

2.5.12. STORE REFerence

The instrument is in this mode when the pushbutton COMPARE is depressed and the pushbutton STORE REF. is pressed.

New captured data is transferred from the input memory into the reference memory. The two blocks of data are compared on a bit-by-bit basis.

2.6. OSCILLOSCOPE MODE

In this mode, the PM 3540 can be used as a general purpose dual-channel oscilloscope.
Due to the interactive relationship between the analyzer and the oscilloscope, it is possible to trigger both sides of the instrument from the same pre-selected triggerword.

2.7. SELECTION OF THE OSCILLOSCOPE MODE

With pushbutton LSA/OSC in the released position, the oscilloscope mode is selected and all controls and sockets of the oscilloscope part of the PM 3540 are available for use.

2.7.1. Input coupling (AC/DC, 0)

AC coupling (pushbutton depressed) is useful to block the d.c. component of a signal. Choice of AC limits the lower frequencies, causing low repetition rate sinewave signals to be attenuated and low repetition rate square-waves to be distorted. The degree of attenuation is determined by the input RC time (0.1 s). Input RC time is extended by 10 if 10:1 passive probes are employed.
When switching to AC coupling it will take approximately five times the RC time before the trace is stabilised to the average value of the input signal.
AC position measurements cannot be made with respect to ground.

0 position disconnects input source and short-circuits input of amplifier to provide zero signal check.

DC coupling (pushbutton released) provides for full range frequency input, i.e. down to d.c.

2.7.2. Use of probes (see also section 3, "INFORMATION CONCERNING ACCESSORIES")

1:1 passive probes should be used for d.c. and low frequencies.
Capacitive loading attenuates high frequencies or increases the rise-time of measurement signals (dependent on source impedance).

10:1 passive probes have less capacitive loading, usually about 10 pF to 20 pF, FET probes are superior, especially when measurements are to be taken from high impedance test points or at the upper frequency limit of the logic-scope bandwidth.

10:1 passive probes must be properly compensated before use. Incorrect compensation leads to pulse distortion or amplitude errors at high frequencies.
For correct adjustment, the CAL output connection can be used (see Fig. 2.9.).

2.7.3. Adjustment of attenuator probes

- Connect the compensation box to the Y_A or Y_B input socket and place the tip of the probe on socket CAL.
- Insert a small screwdriver through the hole in the compensation box and adjust the trimmer to obtain a correct display as shown in Fig. 2.9.

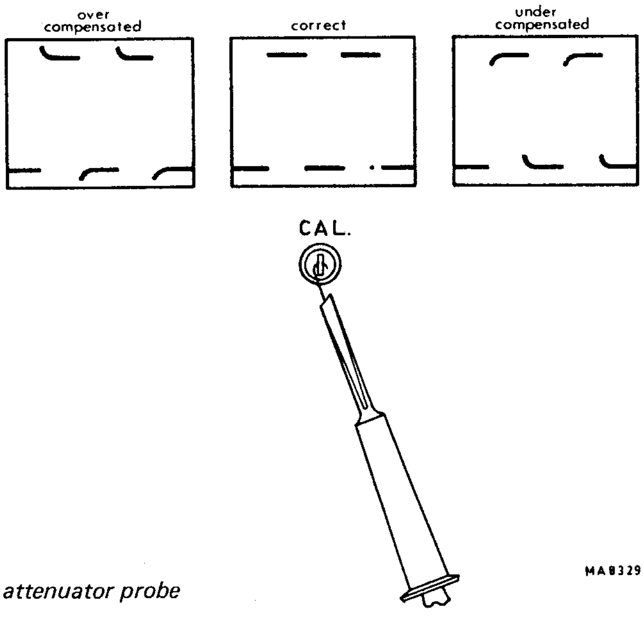


Fig. 2.9. Adjusting an attenuator probe

2.7.4. Selection of chopped or alternate modes

(A, ALT, CHOP, ADD, B)

In dual channel operations (CHOP or ALT depressed) the chopped mode (depress CHOP) must be selected for relatively slow sweep speeds (from .1 ms/div to .5 s/div) or at low repetition rates of sweeps occuring, even at high sweep rates. Selection of the ALTernate mode under these circumstances would make comparisons between waveforms difficult because traces would actually appear to be written one by one. However, when the display is fast enough to be interrupted by the chopping frequency the alternate mode must be selected (depress ALT), usually at sweep rates faster than .1 ms/div.

2.7.5. Differential mode

The A-B mode can be selected by depressing ADD and pulling the channel B POSITION control.
In measurements where signal lines carry substantial common mode signals (e.g. hum) the differential mode will cancel out these signals and leave the remainder (A-B). The capability of the logic-scope to suppress common mode signals is given by the CMR factor (see Fig. 2.10).
To obtain the degree of common mode rejection specified, channel A and B gain must first be equalised.
This can be done by connecting both channels to the CAL output connector, and adjusting one of the continuous controls with the AMPL/DIV switch for minimum deflection on the screen.
When passive 10:1 probes are used a similar equalisation process is recommended by adjusting their compensating controls for minimum deflection.

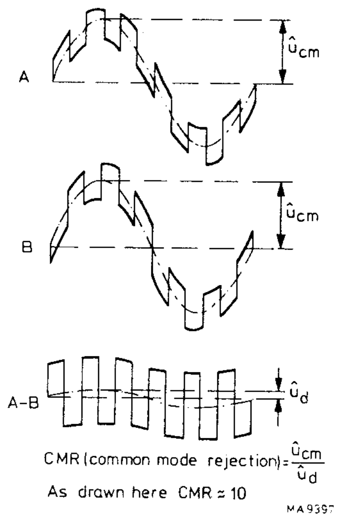


Fig. 2.10. Suppression of common mode signals

2.7.6. Trigger source selection

The trigger source is selected by the front-panel TRIG or X DEFL pushbuttons (S16).

A B EXT DATA
└COMP┘ └QUAL┘

- **Internal triggering** will be most commonly used because it requires only one signal (the Y_A or Y_B input signal) to obtain stable triggering.
- **External triggering.** When tracing many signals it is advantageous to use an external signal for triggering. There is no need to set and reset the trigger controls (LEVEL, SLOPE and SOURCE) on changing the input signal.
  Furthermore the two Y_A or Y_B inputs remain free for examining waveforms.
- **Selection of trigger source.** In comparing synchronous waveforms, that have unequal repetition rates, always select the signal, that has the lowest repetition rate as the trigger source. Not doing so may lead to double pictures (chopped mode) or untrue time-shifts (alternate mode).

- **Composite triggering.** With internal triggering signals are obtained from either the A channel, the B channel preamplifier stages or, when COMP is selected by depressing both A and B pushbuttons, from the delay line driver stage that follows the electronic channel switch.
  Composite triggering offers three advantages:
  1. In differential mode (A-B measurements) triggering is derived from the differential signal. Triggering is not disturbed by common mode signals.
  2. For one channel operation it is not necessary to switch trigger sources from A to B or vice versa.
  3. In the alternate mode, it is possible to compare signals that are not related in time.

Note: When composite triggering is employed in dual channel operation (alternate mode), and there is only one signal applied (to A or B input), stable triggering cannot be obtained. This is normal since the trigger source is also switched from A to B (see Fig. 2.11.).
When composite triggering is employed in dual channel operation (chopped mode) stable triggering can not be obtained because the system will be triggered by the chopped signal transients.

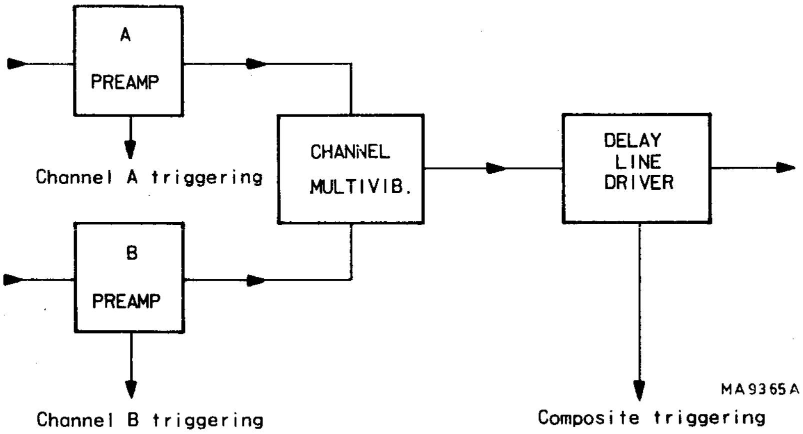


Fig. 2.11. Block diagram of composite trigger circuit

- **Data triggering.** By setting the trigger word to a known logic state that occurs just before a fault in the data stream arises, the oscilloscope's timebase can be triggered so that the instrument only displays the real-time behaviour of two selected signals (input via Y_A and Y_B) just after the defined logic state occurs.
  To do this, you must set the correct triggerword and run in oscilloscope mode with the DATA pushbutton depressed. You can then examine the detailed time-dependent behaviour of any two selected signals at the precise time when a fault is known to occur.
- **Qualifier triggering.** By operating with both DATA and EXT pushbuttons depressed i.e. the QUALifier mode, you can cause triggering to occur only when a triggerword match coincides with a "high" trigger qualifier logic level.
  An unconnected trigger qualifier input is treated as permanently "high".

Note: When measurements in the DATA or QUALifier mode are made. DC and + Slope positions of the trigger mode switch S_2 (see Fig. 2.2.) are strongly recommended.

2.7.7. Selection of trigger mode

(AUTO, AC, DC, TV, +/–)

The AUTO mode is useful because it provides trace(s) on the screen even in the absence of trigger signals. Furthermore, for a signal amplitude larger than 1 division, this mode provides stable triggering independent of the position of the LEVEL control; its range is automatically adjusted to the peak-to-peak value of the signal selected for triggering.

In this way the setting of the LEVEL control is facilitated at low amplitudes of the trigger signal.

The AUTO mode cannot be employed for signals with low repetition rates (10 Hz or lower) because the sweeps would be able to free run in between triggers. Therefore, for low repetition signals normal triggering must be used (AC or DC depressed).

In normal triggering, sweeps are only initiated with a trigger signal applied and the LEVEL control set appropriately.

With AC or DC depressed the range of the LEVEL control is fixed (+ or – 8 divisions or more at the extremes of the LEVEL control with respect to mid screen).

The DC component in the trigger signal can be blocked by depressing AC. This is useful when triggering must take place on a.c. signals superimposed on a large d.c. level.

With AC coupling, the level at which the display starts will change with alterations in the average value of the trigger signal. The trigger level is thus no longer referenced to signal ground. This may cause instability with waveforms that vary in time interval from cycle to cycle. Normally it is preferable to use the DC position.

Slope selection is made with pushbutton +/–. In TV mode – must be selected for negative video signals and + for positive video signals. The LEVEL control is inoperable in the TV mode.

No buttons depressed offers an extra mode of use, a trace is on screen in the absence of a trigger signal, but the LEVEL range is fixed.

2.7.8. Time-base magnifier

The magnifier is operated by pulling the switch incorporated in the X position control.

When this switch is in the x10 position, the time-base sweep speed is increased 10 times. The sweep time is therefore determined by dividing the indicated TIME/DIV value by 10.

2.7.9. XY Measurements

XY measurements are made with the TIME/DIV switch at X DEFL, the source of horizontal deflection being selected by the EXT X DEFL or TRIG pushbutton switch (S16).

XY measurements provide a useful means of making frequency or phase shift comparisons by displaying Lissajous patterns.

Measurements can be made up to 100 kHz with less than 3° phase error between oscilloscope channels.

The sensitivity for the different XY modes is shown in the following table:

X DEFL	SENSITIVITY
A	AMPL/DIV A ± 10 %
B	AMPL/DIV B ± 10 %
EXT	0.5 V/div
DATA	For this mode, not applicable.

2.8. PROCEDURES REQUIRED FOR THE REMOVAL OF FUSES, BEZEL AND CONTRAST PLATE

2.8.1. Removing the instrument covers

Always ensure that the mains supply is disconnected before removing any instrument cover plates.
The instrument is protected by three covers: a front panel protection cover, a wrap-around cover with carrying handle, and a rear panel.
To facilitate removal of the wrap-around cover and the rear panel, first ensure that the front cover is in position.

Then proceed as follows:

- Hinge the carrying handle clear of the front cover; to this end, push both pivot centre buttons (Fig. 2.12.)
- Stand the instrument on its protective front cover on a flat surface.
- Slacken the two coin-slot screws located on the rear panel.
- Lift the rear panel and unplug the connector on the power supply board.
- Lift off the wrap-around cover.
- For access to the front-panel, stand the instrument horizontally and snap off the front cover.

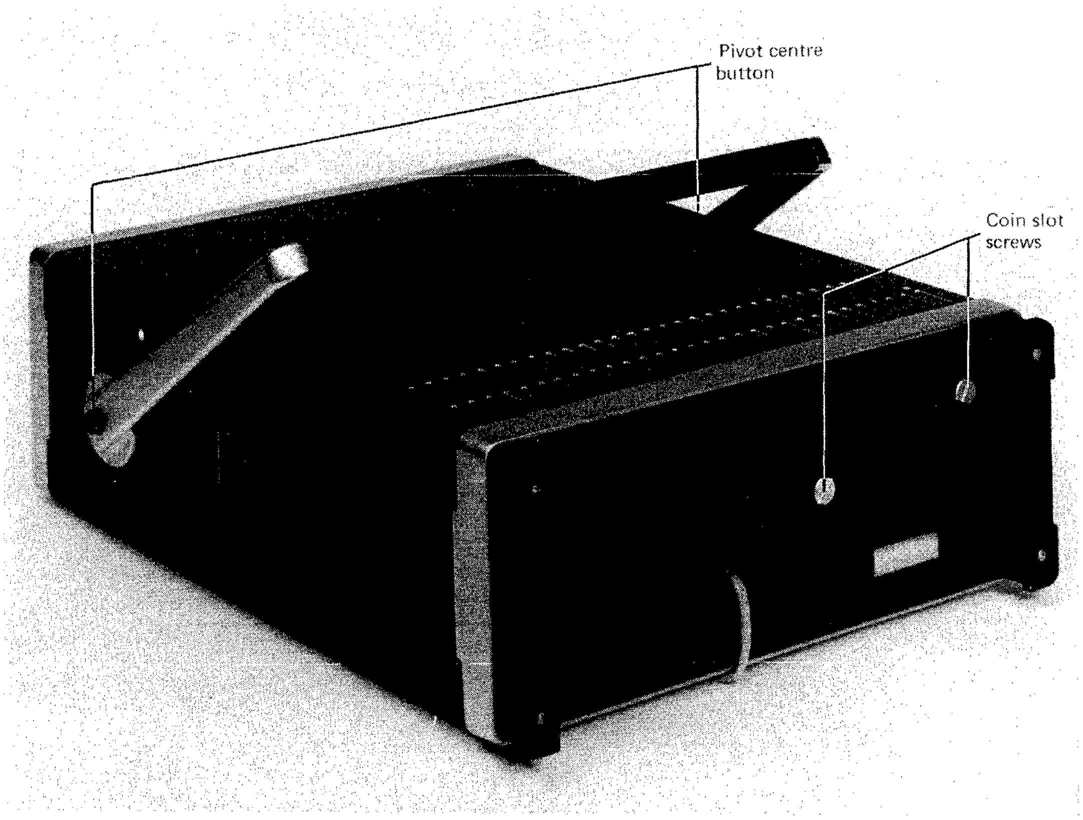


Fig. 2.12. Removing the instrument covers

2.8.2. Removing the mains transformer

- Remove wrap-around cover and rear panel (section 2.8.1.).
- Take the lid off the voltage adapter compartment after removing the 4 cross-slotted screws.
- Remove the 4 cross-slotted screws that hold the lid of the transformer compartment.
- Lift the lid with the attached transformer, simultaneously sliding the wire form between transformer and voltage adapter out of the slit in the transformer compartment.
- The transformer and thermal fuse are then accessible for replacement.

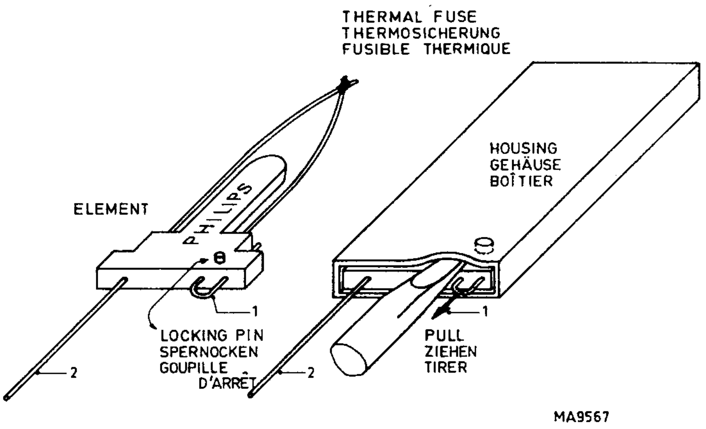

THERMAL FUSE
THERMOSICHERUNG
FUSIBLE THERMIQUE
HOUSING
GEHÄUSE
BOÎTIER
ELEMENT
PHILIPS
1
LOCKING PIN
SPERNOCKEN
GOUPILLE D'ARRÊT
2
2
1
PULL
ZIEHEN
TIRER
MA9567

Fig. 2.13. Replacing the thermal fuse

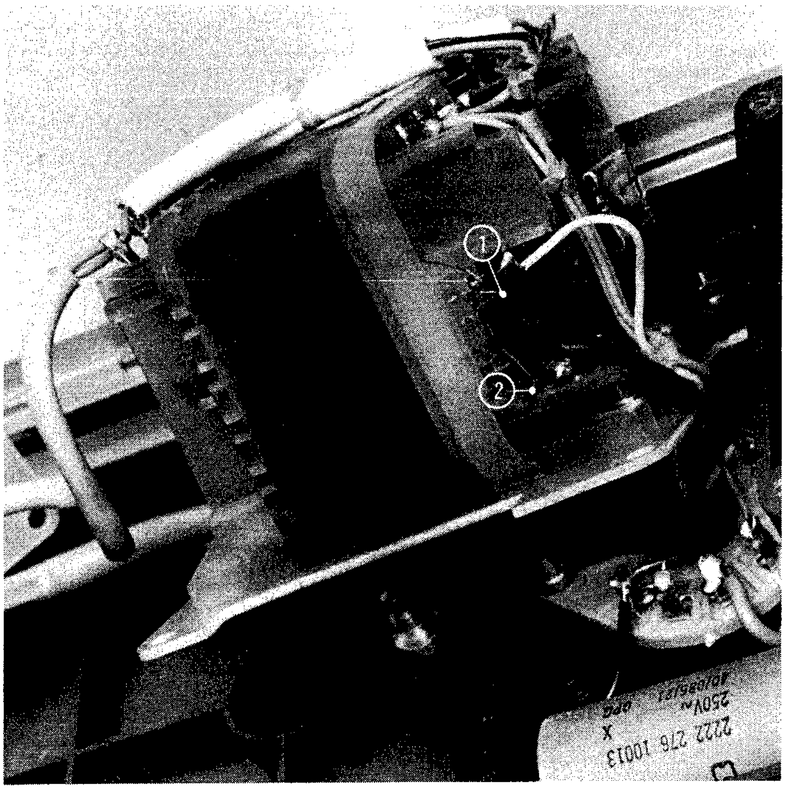


Fig. 2.14. Replacing the thermal fuse

2.8.3. Replacing the thermal fuse F101

- Remove the mains transformer (section 2.8.2.).
- Unsolder fuse terminals 1 and 2 (Fig. 2.13. and 2.14.).
- Only the fuse wire of the old fuse is replaced and not the complete fuse; to this end, bend the housing of the fuse slightly outwards, disengage the locking pin and pull out the wire.
- Take the new fuse and remove the fuse wire out of its housing in the same way as described above.
- Push the new fuse wire into the housing of the old one until the locking pin snaps into the hole. The loop in the fuse wire must point to terminal 1.
- Solder the fuse wire to terminals 1 and 2.

2.8.4. Replacing the fuse F201

- Remove wrap-around cover and rear panel (section 2.8.1.).
- Fuse F201, which is located on the power supply printed circuit board, is now accessible for replacement.

2.8.5. Removing the bezel and the contrast plate

- Take hold of the bezel's bottom corners and gently pull it from the front panel (Fig. 2.15.).
- The contrast filter can be removed by pressing it gently out of the bezel.

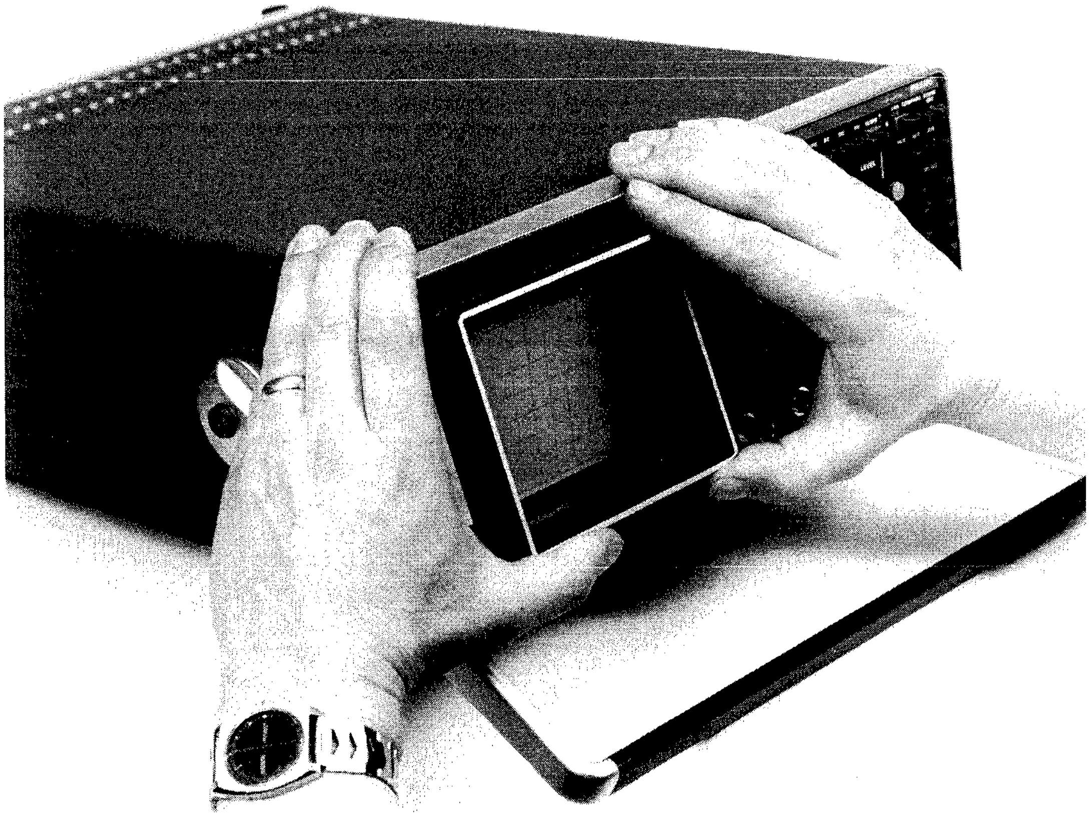


Fig. 2.15. Removing the bezel and the contrast plate

2.9. MAINTENANCE

This instrument generally requires very little maintenance, as the instrument has no components that are subject to wear. However, to ensure reliable and troublefree operation, the instrument should not be exposed to moisture, heat, corrosive elements or excessive dust.

The appearance of the wrap-around cover, lacquered with Nextel suede coating will deteriorate after some time. To clean it, use a soft cleansing pad with some ethanol or common household cleaning detergent. Abrasive cleaning pads or materials should not be used, otherwise surface scratches will result.

WARNING: The Nextel suede coating is ethanol-resistant, but is susceptible to methylated spirit, which will attack the surface (due to one of the de-naturing substances).

Cleaning the front and rear panels; do not use chemical solutions such as trichlorethylene or acetone.
Use a soft pad, cloth or cotton-wool with some water and common household cleansing or some alcohol or white spirit.

Check that after long periods of use, the holes in the cabinet plates don't get stopped up with dust. If necessary use pressurized air to clear the holes.

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1. Allgemeines

1.1. EINLEITUNG

Das Logik-Skop PM 3540 ist ein kompaktes, tragbares Gerät, ausgelegt nach ergonomischen Gesichtspunkten und im Besitze vielseitiger Messmöglichkeiten. Das Logik-Skop ist eine Kombination eines 16-Kanal Hochleistungs-Logik Zustands-Analysators und eines hochwertigen 25 MHz Zweistrahl Oszilloskops. Dank dieser Kombination lassen sich mit Hilfe dieses Gerätes die unterschiedlichsten digital arbeitenden Systeme testen. Dies gilt sowohl im Datenbereich wie im Zeitbereich. Auf dem Gebiet der Daten gestattet der Analysator dem Anwender die Überprüfung von Software zur Lokasierung von Fehlern. Das Oszilloskop hingegen hilft dem Anwender zeitbezogene Schwierigkeiten als mögliche Fehlerquelle zu ermitteln (Hardwarefehler).
Durch die Kombination der Analysator-Oszilloskop Funktionen in einem einzigen Testgerät eignet sich das Gerät für einen breitgefächerten Einsatzbereich in Forschung und Entwicklung, sowie für Produktionstests, Fehlersuche, Wartung, Feldservice und für Lehrzwecke.
Eine Elektronenstrahlröhre deren nutzbare Bildschirmfläche aus 8x10, durch einen Innenraster kalibrierten Teilen besteht, liefert bei Oszilloskopbetrieb zwei präzise Leuchtspuren.
Im Analysatorbetrieb lässt sich die Datenanzeige tabellarisch in binärer, oktaler oder hexadezimaler Form darstellen.
Eine doppelt isolierte Stromversorgung erlaubt direkten Anschluss der Geräte-Erde an erdfreie Schaltungen, vorausgesetzt diese Messerde führt keine berührungsgefährlichen Spannungen.
Interferenzen durch Erdströme, wie sie häufig bei geerdeten Geräten vorkommen, werden ebenfalls wesentlich reduziert.
Der Einsatz des Logik-Skops im Feld wird durch wahlweisen Battereibetrieb ermöglicht.

WARNUNG: **Die Geräte-Erde (und die Tastkopf-Erdleitung) darf nicht mit berührungsgefährlichen Spannungen verbunden werden.**

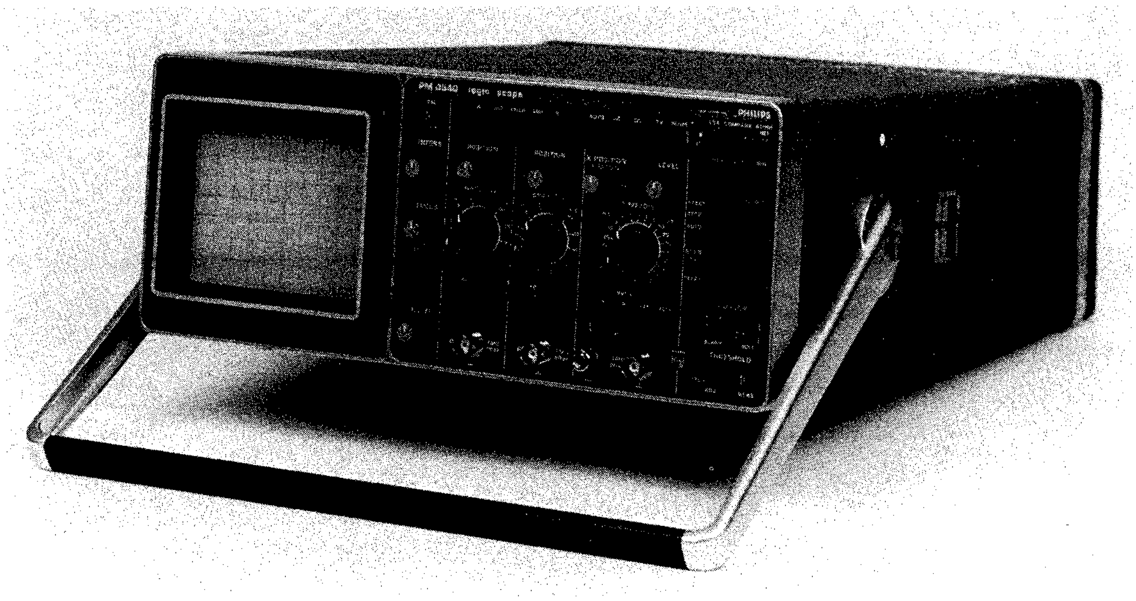


Abb. 1.1. Logik-Skops PM 3540

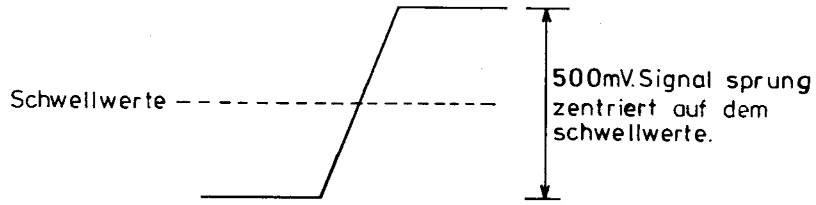

Schwellwerte
500mV.Signal sprung zentriert auf dem schwellwerte.

Abb. 1.2. Minimal erforderliche Signaländerung

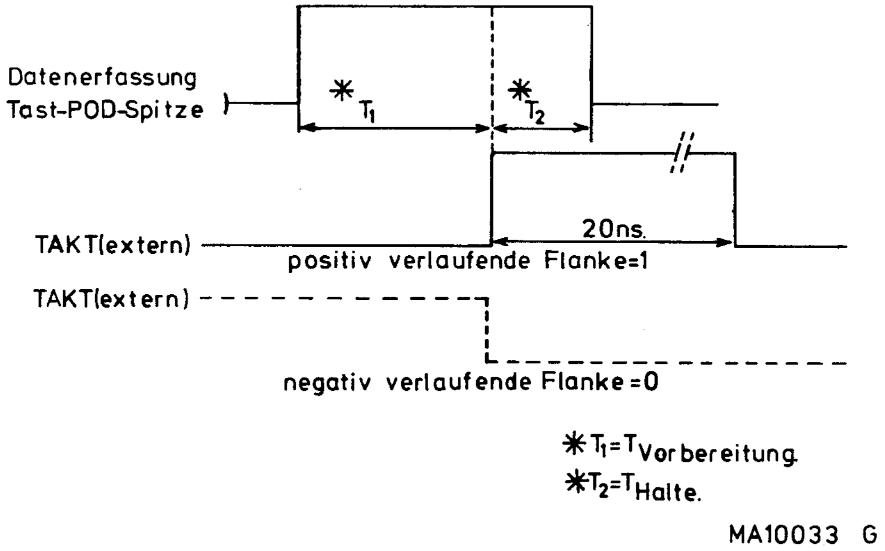

Datenerfassung Tast-POD-Spitze
*T1
*T2
20ns.
TAKT(extern)
positiv verlaufende Flanke=1
TAKT(extern)
negativ verlaufende Flanke=0
*T1=TVorbereitung.
*T2=THalte.
MA10033 G

Abb. 1.3. Definierung von Vorbereitungs- und Halte-Zeit

1.2. TECHNISCHE DATEN

Dieses Gerät ist gemäss IEC 348, Sicherheitsbestimmungen für elektrische Mess- und Regeleinrichtungen gebaut und geprüft und hat das Werk in sicherheitstechnisch einwandfreiem Zustand verlassen. Um diesen Zustand zu erhalten und einen gefahrlosen Betrieb sicherzustellen muss der Anwender die Hinweise und Warnvermerke beachten, die in der vorliegenden Anleitung enthalten sind.
Zahlenwerte mit Toleranzangaben werden bei Umgebungstemperaturen von +5 °C ... +40 °Cgarantiert falls nicht anders angegeben. Zahlenwerte ohne Toleranzangaben sind Durchschnittswerte und dienen nur zur Information. Die gegebenen Kenngrössen gelten nach einer Anwärmzeit des Geräts von 15 Minuten.

BETRIEBSARTEN :
- Logik-Analysator allein
- Oszilloskop allein
- Beide Logik-Analysator und Oszilloskop zusammen, wobei letzteres vom L.A. getriggert wird.

BEMERKUNG :
- Bezüglich Betrieb und Wählverfahren dieser Betriebsarten siehe Abschnitt 2. "GEBRAUCHSANLEITUNG".

1.2.1. Technische Daten des Analysators

1.2.1.1. Analysator Eingänge

: 3 Mehrfach-Steckverbindungen für:
- 16 Datenkanäle (über 2 Steckverbindungen)
- 1 Takt } über 1 Steckverbindung
- 3 Taktqualifizierer

1.2.1.2. Dateneingang

Alle Werte sind typische Werte und an der Tastkopfspitze spezifiziert : Über 3 Tast-Köpfe PM 8820 für je 8 Anschlüsse:
- Tastkopf 1, Kanäle 0 ... 7
- Tastkopf 2, Kanäle 8 ... 16
- Tastkopf 3, Takt und Taktqualifizierer

Impedanz : 4 MΩ // 6 pF

Max. Spannung : –50 V ... +50 V

Schwellwert : TTL, +1.4 V fest
Variabel: von 0 bis +10 V stufenlos einstellbar über Testpunkt auf der Frontplatte messbar.

Max. Empfindlichkeit : 500 mV_{s-s} Signaländerung (siehe Abb. 1.2.)

Vorbereitungs- und Haltezeit : Vorbereitungszeit= 40 ns
Haltezeit = 20 ns
bezogen auf die extern wirksame Taktflanke (siehe Abb. 1.3.)

1.2.1.3. Takt

Quelle : Externer (synchron) Eingang über Tastkopf PM 8820

Schwelle : Entsprechend dem dateneingang

Taktrate : Max. 10 MHz

Taktimpulsbreite : Minimal 20 ns (siehe Abb. 1.3.)

Abtastung (sampling) : Wählbar an positiver oder negativer Taktflanke

1.2.1.4. Taktqualifizierer

Anzahl : 3 Taktqualifizierer (Eingabe über Vielfach-Tastkopf PM 8820)

Schwelle : Entsprechend dem Dateneingang

Abtastung : Erfolgt nur wenn der Taktqualifizierer an der Taktflanke "wahr" ist.

"True" (Wahr) Wahl : "1" für hoch
"0" für niedrig
"X" für "don't care" (ohne Einfluss)

Vorbereitungs- und Haltezeit : Vorbereitungszeit = 20 ns
Haltezeit = 5 ns
bezogen auf die extern wirksame Taktflanke (siehe Abb. 1.3.)

1.2.1.5. Trigger

Quelle : Intern, extern, beides und manuell

Intern : Durch Triggerwort-Erkennung auf 16 Kanälen

Extern : Eingang über die BNC Buchse "EXTERNAL" an der Frontplatte in der Betriebsart QUAL.
Triggerung erfolgt nur wenn der Triggereingang an der Taktflanke "Wahr" ist und das Triggerwort auf "don't care" (x ... x) gesetzt ist.
Der Zustand ist "Wahr" wenn das Eingangssignal über dem Schwellenwert liegt, aber mindestens dem TTL-Pegel entspricht.

Beides (Intern + Extern) : Durch Triggerwort Erkennung auf 16 Kanälen zusammen mit dem Triggerqualifizierer.
Der Triggerqualifizierer Anschluss erfolgt über die BNC Buchse "EXTERNAL" an der Frontplatte in der Betriebsart QUAL.
Der Triggerqualifizierer-Eingang muss an der Taktflanke "Wahr" sein.
Der Zustand ist "Wahr" wenn das Eingangssignal über dem Schwellenwert liegt, aber mindestens dem TTL-Pegel entspricht.

Manuell : Über die START/STOP Drucktaste auf der Frontplatte.

Wählen des Triggerwortes : Durch direkte Ableitung von den gespeicherten Daten mit Hilfe der Drucktaste STORE TRIG.
Der Inhalt des ersten Wortes der Darstellung wird das neue Triggerwort (siehe Abb. 2.5.).
Durch Wahl über die Bildschirm-Textzeilen mit Hilfe des Cursors und der Bedienungselemente 1/+, X und 0/— im erforderlichen Format (Hex. Oct oder Bin).

Triggerverzögerung : Triggerung kann um 0 ... 9999 Taktimpulse verzögert werden eingestellt über den Bildschirm und Wahltasten + und —.
Triggerverzögerung Ein-/Ausschaltung durch Drucktaste.

1.2.1.6. Start

Quelle : Automatisch oder manuell

Automatisch : Das Gerät startet automatisch nach einer Darstellungszeit von etwa 1 Sekunde um Pseudo-Echtzeit Beobachtungen zu ermöglichen.

Manuell : Über START/STOP Drucktaste auf der Frontplatte.

1.2.1.7. Speicher

: Das Speicherformat ist 64 x 16 Bit-Worte.
Im Vergleichsbetrieb (COMPARE) wird ein zweiter Speicher gleicher Grösse eingesetzt.

1.2.1.8. Darstellung (siehe Abb. 2.5.)

: Elektronenstrahlröhre des Oszilloskops (Technische Daten sind 1.2.2.1. zu entnehmen).
Im oberen Teil des Bildschirms werden Textzeilen dargestellt, die Parameter und den Zustand des Geräts angeben.
Anzeige der Zeilennummer.
Das Triggerwort wird bezeichnet mit TRIG und ist Zeilennummer 0.
Alle anderen Zeilen werden bezogen auf das Triggerwort nummeriert.
Das gilt auch für den verzögerten Betrieb.
Der Cursor (in den Textzeilen) lässt sich horizontal und vertikal bewegen.
Spaltenunterdrückung (BLANK) und Zeilenverschiebung (ROLL) Möglichkeit.

Anzeigearten : Zustandstabellen-Format in Binär, hexadezimal oder oktal.
Binär wird die Zustandstabelle in 16 Worten von 16 Bits angezeigt.
Die 16 Bits sind in 4 Gruppen von je 4 Bits angeordnet.
Bei hexadezimaler und oktaler Betriebsart werden Zustandstabelle und Triggerwort neu gruppiert.

1.2.2. Technische Daten des Oszilloskopteils

Einschliesslich der kombinierten Analysator/Oszilloskop-Funktionen mit den Triggerquellen:

- Y_A, Y_B (COMPosite) und Extern (EXT)
- Data und Qual (über Analysator).

	Bezeichnung	*Beschreibung*	*Nähere Angaben*
1.2.2.1.	*Elektronenstrahlröhre*		
	Typ	D14-125 GH	Rechteckröhre mit Netzelektrode
	Nutzbare Bildschirmfläche	8 x 10 Teile	1 Teil entspricht 1 cm mit 2 mm Unterteilungen entlang der mittleren Achsen
	Bildschirmtyp	P31 (GH)	P7 (GM) wahlweise
	Gesamtbeschleunigungsspannung	10 kV	
	Raster	Innerraster	Stufenlos einstellbare Rasterbeleuchtung
1.2.2.2.	*Vertikalverstärker*		
	Darstellungsarten	Kanal A allein	
		Kanal B allein	
		A und B gechopped	Gechopped mit etwa 500 kHz
		A und B alternierend	
		A und B addiert	
	Kanal B Polarität	Normal oder invertiert	
	Kennlinie:		
	Frequenzbereich	DC : 0 ... 25 MHz (–3 dB) AC : 2 Hz ... 25 MHz (–3 dB)	
	Anstiegszeit	14 ns	
	Impulsverformungen	± 3 % (4 % Spitze-Spitze)	Gemessen bei 8 Teilen Amplitude und einer Signal-Anstiegszeit von ⩾ 1 ns
	Ablenkkoeffizienten	2 mV/Teil ... 10 V/Teil	1-2-5-Folge
	Stufenloser Einstellbereich	1 : ⩾ 2,5	Unkalibriert
	Ablenk-Fehlergrenze	± 3 %	
	Eingangsimpedanz	1 MΩ/20 pF	
	Zeitkonstante der Eingangsschaltung	0,1 s	Kopplungsschalter auf AC
	Maximal zulässige	400 V	Gleichspannung + Spitzenwert einer Wechselspannung
	Vertikale Strahlverschiebung	16 Teile	
	Dynamischer Bereich	24 Teile	
	Sichtbare Signalverzögerung	40 ns	
	Gleichtaktunterdrückung in A-B Betrieb	⩾ 40 dB bei 1 MHz	Nach Einstellung bei Gleichspannung oder niedrigen Frequenzen
	Übersprechen zwischen Kanälen	–40 dB oder besser bei 10 MHz	
	Instabilität des Leuchtflecks:		
	Temperaturdrift	⩽ 0,3 Teil/Stunde	

	Bezeichnung	*Beschreibung*	*Nähere Angaben*
1.2.2.3.	*Zeitablenkung*		
	Zeitkoeffizienten	0,5 s/Teil ... 0,2 µs/Teil	1-2-5 Folge
	Kontinuierlicher Einstellbereich	1 : ⩾ 2,5	Nicht kalibriert
	Fehlergrenze des Koeffizienten	± 3 %	
	Dehnung	x10	
	Fehlergrenze der Dehnung	± 2 %	
1.2.2.4.	*Triggerung*		
	Quelle	Extern	Triggerung über Eingangsbuchse "External" auf der Frontplatte
		Intern	Triggerung über Oszilloskop Triggerung über Analysator
		Intern + Extern	Triggerung über Analysator und Eingangsbuchse "External" auf der Frontplatte
	Triggerung über Oszilloskop	Y_A und Y_B und zusammengesetzt (COM-Posite)	Bei COMP ist Taste A & B eingedrückt.
	Triggerung über Analysator	Auf Triggerwort	Taste DATA gedrückt
	Triggerung über Analysator + Extern	Auf Triggerwort und Triggerqualifizierer	In Betriebsart QUAL (Taste EXT & DATA gedrückt) und Trigger qualifizierer "wahr" (true). "Wahr" ist bei Pegel "hoch".
	Triggerbetriebsarten	Automatisch, normal Wechselspannung, normal Gleichspannung und TV	TV-Zeile oder Bild geschaltet mit Schalter TIME/DIV TV-Zeile: 2 µs/Teil ... 20 µs/Teil TV-Bild: 50 µs/Teil ... 5 s/Teil
	Trigger-Empfindlichkeit	Intern: 1,0 Teil bei 25 MHz oder Worttriggerung Extern: 0,5 V Spitze-Spitze bei 25 MHz	
		TV int : 0,7 div	Sync. Impuls Ampl.
		TV ext : 0,35 V Spitze-Spitze	Sync. Impuls Ampl.
	Triggerfrequenzbereich	AUTO : 20 Hz ... ⩾ 25 MHz AC : 5 Hz ... 25 MHz DC : 0 Hz ... 25 MHz	Durchschnittlich ist stabile Triggerung noch erreichbar bei 50 MHz und 2 Teilen oder 1 Vss Amplitude
	Pegelbereich	AUTO : Proportional dem Spitze-Spitze Wert des Triggersignals	
		AC, DC : 16 Teile bei interner Triggerung und 8 V bei externer Triggerung	+ oder −8 Teile und + oder −4 V bezogen auf Bildschirmmitte
	Triggerflanke	Positiv oder negativ gehend.	
	Eingangsimpedanz (Externe Buchse)	1 MΩ // 20 pF	
	Maximal zulässige Eingangsspannung (Externe Buchse)	400 V DC+AC-Spitze-Spitze für QUAL-Betrieb ± 50 V	

1.2.2.5. X-Ablenkung

Quelle	A, B oder EXT	Je nach Einstellung des Triggerquelle-Schalters, wenn Schalter TIME/DIV in Stellung X DEFL.
Ablenkkoeffizienten	A oder B, wie eingestellt mit AMPL/DIV Schalter EXTERNAL: 0,5 V/div	
Ablenk-Fehlergrenze	± 10 % in A oder B	
Frequenzbereich	Gleichspannungskopplung 0 ... 1 MHz (–3 dB) Wechselspannungskopplung 5 Hz ... 1 MHz (–3 dB)	
Phasenverschiebung	≤ 3° bei 100 kHz	
Dynamischer Bereich	24 Teile	Für Frequenzen ≤ 100 kHz

1.2.2.6. Kalibriergenerator

Ausgangsspannung	1,2 V Spitze-Spitze	Rechteckspannung
Fehlergrenze	± 1 %	
Frequenz	≈ 2 kHz	

1.2.3. Technische Daten der Stromversorgung

Bezeichnung	*Beschreibung*	*Nähere Angaben*
Wechselspannungsversorgung	Doppelt isoliert	Schutzklasse II, IEC 348
Normaler Spannungsbereich (am Netzspannungsumschalter)	110, 127, 220, oder 240 V (± 10 %)	Wechselspannung
Nominaler Frequenzbereich	46 ... 440 Hz ± 10 %	
Leistungsaufnahme	45 W max.	Bei Netz-Nennspannung
Gleichspannungsversorgung		
Spannungsbereich	23-27 V Gleichspannung	Erdfreier Eingang
	22-28 V Gleichspannung	Bei eingeschränkten Spezifikationen
Stromverbrauch	1,35 A max.	
Kapazität gegen Erde	110 pF	Gemessen mit Gummifüssen auf einer geerdeten 1 m2 grossen Metallplatte
	23 pF	Gemessen 30 cm über einer geerdeten 1 m2 grossen Metallplatte

1.2.4. Einflussgrössen

Die angegebenen Daten gelten nur dann, wenn das Gerät gemäss den offiziellen Prüfverfahren kontrolliert wurde. Einzelheiten, die dieses Verfahren und die Fehlergrenzkriterien betreffen, können von der PHILIPS Organisation Ihres Landes oder von der N.V. PHILIPS' GLOEILAMPENFABRIEKEN TEST AND MEASURING DEPT., EINDHOVEN, NIEDERLANDE angefordert werden.

Umgebungstemperaturbereich:

Nominaler Betriebsbereich	+5 °C ... +40 °C
Betriebsgrenze	–10 °C ... +55 °C
Lagerung und Transport	–40 °C ... +70 °C
Feuchtigkeit	Entspricht den IEC 68 Db Bedingungen
Stossfestigkeit	1000 Stösse je 10 g. 1/2 Sinus, Dauer 6 ms in jeder der 3 Richtungen

Bezeichnung	*Beschreibung*	*Nähere Angaben*
Vibration	30 Minuten in jeder der 3 Richtungen, 10-150 Hz, 0,7 mm Spitze-Spitze und 5 g max. Beschleunigung	
Höhe:		
Betriebsgrenze	5000 m (im Freien)	ist 475 mbar oder 47,5 kPa
Transportgrenze	15000 m (im Freien)	ist 100 mbar oder 10,0 kPa
Erholungszeit	30 Minuten wenn die Temperatur des Gerätes von −10 °C auf +20 °C erhöht wird, bei 60 % relativer Luftfeuchtigkeit	
Störgrad	Das Gerät entspricht den Anforderungen gemäss VDE, Störgrad K	

1.2.5. Mechanische Daten

Abmessungen:		
Länge	445 mm	Ohne Handgriff und Bedienungselemente
Breite	335 mm	Ohne Handgriff
Höhe	137 mm	Ohne Füsse
Gewicht	8 kg	

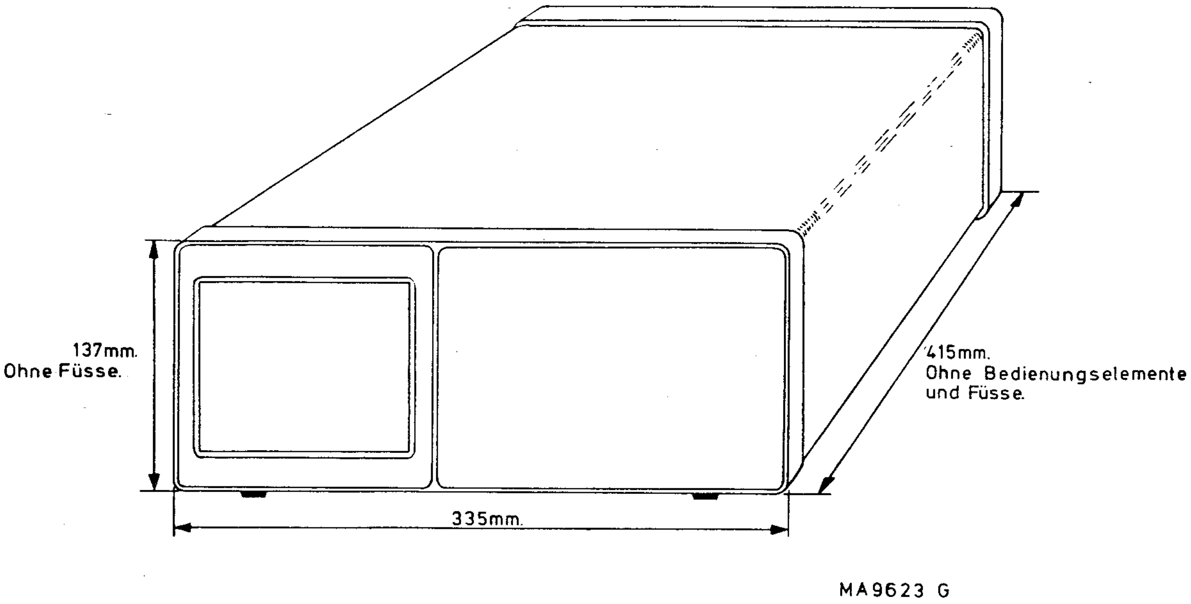

137mm.
Ohne Füsse.
415mm.
Ohne Bedienungselemente und Füsse.
335mm.
MA9623 G

Abb. 1.4. Abmessungen

1.3. ZUBEHÖR

1.3.1. Mitgeliefert

1 Abdeckhaube
1 BNC 4 mm Adapter
2 Tastköpfe PM 8925
1 Bedienungsanleitung
3 Mehrfach-Tastköpfe PM 8820

1.3.2. Wahlzubehör (siehe auch Abschnitt 3 "Einzelheiten betreffend Zubehören")

Tastköpfe für den Analysator	Mehrfach-Tastkopf	PM 8820
	Erweiterungssatz für PM 8820	PM 8819
	Qualifizierer-Erweiterungstastkopf	PM 8810
Oszilloskop-Tastköpfe	Passiver Tastkopf 1:1 (1,5 m) 15 MHz	PM 8921
	Passiver Tastkopf 1:1 (2,5 m) 15 MHz	PM 8921L
	Passiver Tastkopf 10:1 (1,5 m) 40 MHz	PM 8925
	Passiver Tastkopf 10:1 (2,5 m) 40 MHz	PM 8925L
	Passiver Tastkopf 10:1 (1,5 m) 75 MHz	PM 8927
	Passiver Tastkopf 100:1 (1,5 m) 5,6 kV	PM 8927L
	Passiver Tastkopf 100:1 (1,5 m) 5,6 kV	PM 8932
	Isolierverstärker	PM 8940
	FET Tastkopf 1:1, 10:1 und 100:1	PM 8943
	Stromzange	PM 9355
Verschiedenes	Oszilloskop-Rolltisch	PM 8991
	Polaroidfilter	PM 8910
	Lichtschutztubus	PM 9366
	Langer Lichtschutztubus	PM 8980
	Oszilloskopkamera	PM 9381
	Adapter für PM 9381	PM 8972
	19" Gestelleinbau	PM 8963
	Zubehörtasche	PM 8992
	BNC-Adapter	PM 9051
	Abgleichbesteck	800/NTX
	Batteriespeiseteil	PM 8901

2.Gebrauchsanleitung

2.1. ALLGEMEINES

Dieser Abschnitte enthält eine Beschreibung der für die Installierung des PM 3540 erforderlichen Verfahren und Sicherheitsmassnahmen, zeigt und erläutert in Kürze die Funktion von Bedienelementen und Hinweisen auf Frontplatte und Rückwand, und erklärt die praktischen Aspekte des Betriebs, so dass der Anwender die Hauptfunktionen des Geräts rasch bewerten kann.

2.1.1. Sicherheitsvorschriften (den IEC348 Bedingungen entsprechend)

Vor Anschluss des Geräts an das Netz ist eine Sichtkontrolle des Geräts vorzunehmen, um festzustellen ob das Gerät möglicherweise während des Transports beschädigt wurde. Wenn irgend welche Defekte wahrgenommen werden darf das Gerät nicht an das Netz angeschlossen werden.
Vor Wartungs- oder Reparaturarbeiten ist das Gerät von allen Stromquellen zu trennen und müssen alle Hochspannung führenden Teile entladen sein. Wenn danach eine Kalibrierung, Wartung, oder Reparatur am geöffneten Gerät unter Spannung unvermeidlich ist, so darf das nur durch eine Fachkraft, die die damit verbundenen Gefahren kennt, geschehen. Im Normalbetrieb erübrigt die doppelte Isolierung der Stromversorgung die Notwendigkeit einer Schutzerde.
Es ist zu beachten, dass Kondensatoren im Gerät noch geladen sein können, selbst wenn das Gerät bereits von allen Spannungsquellen getrennt ist.
Eine Leiterplatte darf erst dann entfernt werden, wenn das Gerät mindestens 1 Minute ausgeschaltet ist.
Wenn ein Gerät von kalter in warme Umgebung gebracht wird, kann Kondensation einen sicherheitsgefährdenden Zustand hervorufen.
In einem solchen Falle muss man dem Gerät etwa 30 Minuten (siehe Erholungszeit unter "Einflussgrössen 1.2.4) Zeit zur Anpassung an die Umgebung geben, bis alle Kondensation verdampft ist.

WARNUNG: **Es ist zu beachten dass bei allen Messungen die Gehäuseerde des Geräts die gleiche Spannung wie die Tastkopferde erreicht.
Weder die Tastkopferdleitung noch die Gehäuseerde dürfen mit berührungsgefährlichen Spannungen verbunden werden.**

2.1.2. Örtlicher Netzanschluss und Sicherung

Vor dem Anschliessen an das Netz ist zu prüfen, ob das Gerät für die örtliche Netzspannung eingestellt ist. Das Gerät wird eingestellt auf 220 V geliefert. Falls das Gerät mit einem 110 V, 127 V oder 240 V Netz verwendet wird, ist die geeignete Netzspannung mit Hilfe des Spannungsumschalters und der Geräterückwand so einzustellen dass er die erforderliche Spannung anzeigt (siehe Abb. 2.1).

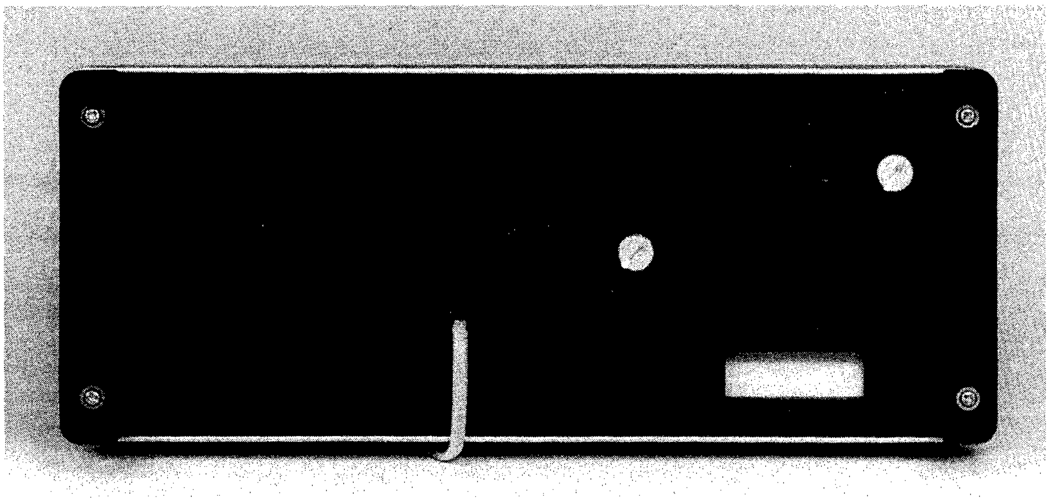


Abb. 2.1. Rückseite des Logik-Skops PM 3540 mit Ansicht des Spannungsumschalters

2.1.3. Sicherung

Das Gerät ist durch eine zwischen den Wicklungen des Netztransformators angebrachte Thermosicherung gegen Überlastungen geschützt. Die Sicherung lässt sich nach Abnahme der Rückwand ersetzen (siehe Abschnitt 2.8.). Es dürfen nur Sicherungen des vorgeschriebenen Wertes benutzt werden.

2.1.4. Anschluss an eine externe Stromversorgung

Eine externe Stromversorgung oder Batterie von 23 V bis 27 V mit einer Mindestleistung von 2 A kann mit der Buchse an der Geräterückwand verbunden werden (Gleichspannungs-Anschlusskabel 4822 321 20125).
Der Innenleiter muss an den Minuspol und der Aussenleiter an den Pluspol angeschlossen werden, wie an der Rückwand angegeben.
Gegen Überlastungen und Polaritätswechsel ist das Gerät durch eine interne Sicherung und Diode geschützt.
Die Sicherung lässt sich nach Abnahme der Gehäuserückwand ersetzen (siehe Abschnitt 2.8.).

2.1.5. Abdeckhaube und Betriebslage

Die Abdeckhaube lässt sich auf einfache Weise durch Ziehen von der Gerätefront abnehmen.
Das Gerät darf in waagrechter Lage oder mit Hilfe des Tragbügels als Kippbügel in verschiedenen Schrägstellungen aufgestellt werden.

2.1.6. Tragbügel

Der Tragbügel lässt sich drehen wenn die Lagerzapfenknöpfe eingedrückt werden.

2.1.7. Einschalten

Der Schalter POWER ist gekoppelt an den Rasterbeleuchtungs-Einsteller ILLUM, gleich neben dem Bildröhrenrahmen. Die zugehörige Signallampe POWER ON/OFF befindet sich neben Einsteller ILLUM.
Das Gerät darf niemals eingeschaltet werden wenn eine Leiterplatte ausgebaut ist.

2.1.8. Kühlung

Es ist darauf zu achten, dass der natürliche Luftstrom durch das Gerät, nicht behindert wird. Das Gerät nie auf Wärme erzeugende oder ausstrahlende Oberflächen stellen.
Keine anderen Geräte oder Papiere auf das Gerät legen, um übermässige Erwärmung zu vermeiden.

2.2. BEDIENUNGSELEMENTE UND BUCHSEN

2.2.1. Bedienungselemente und Buchsen des Analysatorteils

2.2.1.1. Betriebsart

Funktionswahlschalter	Zweiweg-Drucktaste
LSA (eingedrückt)	Analysatorbetrieb gewählt
OSC (ausgerastet)	Oszilloskopbetrieb gewählt
Drucktaste COMPARE	Der gespeicherte Datenblock wird mit dem Referenzdaten-Block verglichen
Drucktaste STORE REF	Daten werden von Eingangs-Speicher in den Referenzspeicher übertragen. (Nur wenn Drucktaste COMPARE eingedrückt ist.)

2.2.1.2. Darstellung

Drucktaste HEX	Wahl der Zustandstabelle in hexadezimalem Format
Drucktaste OCT	Wahl der Zustandstabelle in oktalem Format
Drucktaste BIN	Wahl der Zustandstabelle in birärem Format
Kippschalter BLANK S31 (Taste SELECT ausgerastet)	Stellung "rechts": Darstellung von Datenkanälen wird gelöscht, beginnend bei Kanal 15, solange diese Stellung gewählt ist. Stellung "links": Die gelöschten Kanäle werden wieder in entgegengesetzter Richtung wie bei Stellung "rechts" dargestellt.
Kippschalter CURSOR S31 (Taste SELECT eingedrückt)	Dieser Betrieb erlaubt Verschiebung des Cursors zur Parameterwahl.
Cursor (elektronischer Zeiger) ist ein aufgehelltes Digit den Textzeilen	Stellung "rechts": Cursor nach rechts verschieben. Stellung "links": Cursor nach links verschieben.
Kippschalter CURSOR S32 (Taste SELECT eingedrückt)	Dieser Betrieb erlaubt Verschiebung des Cursors zur Parameterwahl.
Cursor ist ein aufgehelltes Digit in den Textzeilen	Stellung "oben": Cursor aufwärts verschieben. Stellung "unten": Cursor abwärts verschieben.
Drucktaste SELECT (Parameterwahl)	Zur Bestimmung von Taktflanke; Triggerqualifizierer, Triggerwort und Verzögerung. Der Zustand der Parameter ist in den Textzeilen der Darstellung angegeben.
Wahltasten	Parametereinstellung.
Kippschalter ROLL S32 (Taste SELECT ausgerastet)	Stellung "oben": Speicherinhalt von 64 Worten wird hinter dem auf dem Bildschirm dargestellten Ausschnitt nach oben "gerollt". Stellung "unten": Speicherinhalt von 64 Worten wird hinter dem auf dem Bildschirm dargestellten Ausschnitt nach unten "gerollt.
"1" Funktion	Drucktaste "1" wählt "wahr" für einen hohen Pegel oder positiv gehende Taktflanke
"0" Funktion	Drucktaste "0" wählt "wahr" für einen niedrigen Pegel oder negativ gehende Taktflanke.
"X" Funktion	Drucktaste "X" wählt "don't care" (ohne Einfluss)
"+" Funktion	Addierfunktion: 0 ... 9. dez., 0 ... F. hex, 0 ... 7. okt.
"–" Funktion	Subtrahierfunktion: 9 ... 0. dez., F ... 0. hex, 7 ... 0. okt.
Drucktaste DELAY	Betätigt die Triggerverzögerung. Mit Drucktasten "+" und "–" wird der Wert der Triggerverzögerung eingestellt "+" zählt aufwärts bis 9999 "–" zählt abwärts.
Drucktaste STORE TRIG	Nach Eindrücken dieser Taste wird der Inhalt der obersten Zeile (d.h. das erste Wort) des dargestellten Speicher Ausschnitts automatisch das neue Triggerwort, einschliesslich der gelöschten Kanäle. Diese Betriebsart nur möglich wenn Drucktaste COMPARE nicht eingedrückt ist.

2.2.1.3. START

Drucktaste START/STOP	Drucktaste mit zwei Funktionen – der erste Tastendruck startet Datenerfassung – der zweite Tastendruck stoppt Datenerfassung
Datenerfassungsart Schalter SINGLE (ausgerastet)	Zweiweg Drucktastenschalter Daten werden in einer Einzelabtastung erfasst
AUTO (eingedrückt)	Daten werden in automatisch wiederholten Abtastungen erfasst.

2.2.1.4. Schwelle

ADJ/TTL (R12/S33)	Schraubendrehereinstellung für variable Schwelle Einstellbar von 0 V bis +10 V. TTL Schwellspannung von +1,4 V fest.
MEAS	Testpunkt für die feste +1,4 V TTL-Spannung oder die eingestellte Schwellspannung

2.2.1.5. Verschiedenes

Y-Position (R13) (Schraubendrehereinstellung)	Potentiometer für die vertikale Verschiebung des Bildes im Analysatorbetrieb.
Eingang X15	Vielfachsteck-Verbindung für die Eingabe der 8 Kanäle niedrigster Ordnung
Eingang X16	Vierfachsteck-Verbindung für die Eingabe der 8 Kanäle höchster Ordnung
Eingang X17	Vielfachsteck-Verbindung für die Eingabe von Takt und Qualifiziersignal.
Eingang X5 ("EXTERNAL")	'BNC' Buchse, Eingang für Qualifizier- oder Trigger-Signal (siehe auch 2.2.2.4.).

2.2.2. Bedienungselemente und Anschlüsse des Oszilloskop-Teils (Einschliesslich der kombinierten Analysator/ Oszilloskop Funktionen)

2.2.2.1. Betriebsart

Funktionswahlschalter	Zweiweg Drucktastenschalter
OSC (ausgerastet)	Oszilloskopbetrieb gewählt
LSA (eingedrückt)	Analysatorbetrieb gewählt.

2.2.2.2. Vertikale Kanäle

Darstellungsart-Schalter	Funktion Fünf Druckschalter zur Einstellung der Darstellungsarten. Wird keine Drucktaste betätigt, dann ist Betriebsart ALT eingeschaltet.
A	Vertikalablenkung durch ein an Eingang von Kanal A gelegtes Signal.
ALT	Die Darstellung wird am Ende jedes Zyklus des Zeitablenksignals von einem Vertikalkanal auf den anderen umgeschaltet.
CHOP	Das Bild wird mit einer Festfrequenz von einem Vertikalkanal auf den anderen umgeschaltet ($f \approx 500$ kHz)
ADD	Vertikalablenkung durch die Summe der Signale von Kanal A und B (oder –B).
B	Vertikalablenkung durch ein an Eingang von Kanal B gelegtes Signal.
POSITION	Stufenlose Einstellung der vertikalen Verschiebung des Bildes.
PULL TO INVERT B	Zug-Druck Schalter kombiniert mit dem POSITION Schalter von Kanal B. When gezogen wird die Kanal B Signalpolarität umgekehrt.

AMPL/DIV (Aussenknopf)	Stufenweise Einstellung des Vertikalablenkkoeffizienten, von 2 mV/div bis zu 10 V/div in 1-2-5-Folge.
AMPL/DIV (Mittelknopf)	Stufenlose Einstellung des Vertikalablenkkoeffizienten. Es ist zu beachten dass der Ablenkkoeffizienten nur dann kalibriert ist, wenn der Mittelknopf in Stellung CAL (ganz nach rechts) steht.
Eingangskopplungsschalter	Signalkopplung; Zweiweg Druckschalter.
AC (eingedrückt)	Kopplung über einen Sperrkondensator.
DC (ausgelöst)	Direkte Kopplung.
0 (eingedrückt)	Verbindung zwischen Eingangsschaltung und Eingangsbuchse unterbrochen und Eingangsschaltung geerdet.
Y_A	BNC-Buchse für Kanal A Eingang.
Y_B	BNC-Buchse für Kanal B Eingang.

2.2.2.3. *Triggerung*

Triggerungsart-Schalter	*Funktion*
	Fünf Drucktasten zum Einstellen der Triggerungsart und der Polariät der Triggerflanke. Wenn keine der Drucktasten betätigt ist, dann ist Betriebsart AUTO gewählt, und der LEVEL Bereich auf einen festen Wert eingestellt.
AUTO	Ein Bild ist sichtbar auch wenn keine Triggersignale vorhanden sind. Der Bereich der LEVEL-Einstellung ist proportional dem Spitze-Spitze Wert des Triggersignals.
AC	Normale Triggerung und fester Bereich der LEVEL Einstellung. Gleichspannungskomponente des Triggersignals ist gesperrt.
DC	Normale Triggerung und fester Bereich der LEVEL Einstellung. Gleichspannungskomponente des Triggersignals wird durchgelassen.
TV	Zeilen oder Bild Synchronisation je nach Stellung des TIME/DIV Schalters (Bild von 5 s/div bis 50 μs/div und Zeile von 20 μs/div bis 2 μs/div).
+/–	Triggerung auf der positiv oder negativ gerichteten Flanke des Signals. In TV muss "–" für negative Videosignale eingestellt werden und "+" für positive Videosignale.
LEVEL	Stufenlose Einstellung des Signalpegels bei welchem das Oszillogram startet.
TRIG OR X DEFL	(siehe TRIG OR X DEFL Quelle Schalter im nachstehenden Abschnitt 2.2.2.4.).

2.2.2.4. *Horizontaler Kanal*

TRIG. oder X-DEFL.	*Funktion*
	4-fache Drucktaste zur Wahl der Triggerquelle oder der Horizontalablenkungsquelle, wenn Schalter TIME/DIV in Stellung X-DEFL steht. Wenn keine der Drucktasten eingedrückt ist, wird Quelle A gewählt
A	Signal, Kanal A entnommen.
B	Signal, Kanal B entnommen.
COMP (sowohl A wie B eingedrückt, nicht wirksam mit X-DEFL.)	Signal ist jenem Kanal entnommen, der mit dem elektronischen Kanalschalter durchverbunden ist. Triggerung geschieht mit den auf dem Schirm dargestellten Signalformen.

EXT	Triggerung oder X-Ablenkung erfolgt mit dem von einer an Eingangsbuchse X5 ("EXTERN") gelegten Spannung entnommen Signal.
DATA	Interne Triggerung mit einem Signal, das den erfassten Daten entnommen ist, wenn das Triggerwort erkannt wird.
QUAL (EXT & DATA sind beide gedrückt)	Interne Triggerung mit einem den erfassten Daten entnommen Signal, wenn das Triggerwort erkannt wird, mit der Zusatzbedingung eines an Eingangsbuchse X5 ("EXTERN") gelegtem Triggerqualifiziersignals.
X POSITION	Stufenlose Einstellung der horizontalen Lage des Bildes, gekoppelt an einen Zug-Druckschalter für 10-fache Dehnung der Horizontalablenkung (Nur wirksam in Betriebsart Oszilloskop.)
TIME/DIV (äusserer Knopf)	Einstellung des Zeitkoeffizienten von 2 µs/div bis 5 µs/div in 1-2-5-Folge. Bestimmt Zeilen- oder Bildtriggerung in TV-Betriebsart. In Stellung X-DEFL wird die Horizontalablenkung vom Schalter TRIG oder X-DEFL bestimmt.
TIME/DIV (mittlerer Knopf)	Stufenlose Einstellung des Zeitkoeffizienten. Muss in Stellung CAL stehen (d.h. ganz nach rechts), damit die Zeitachse gemäss der Anzeige des Schalters TIME/DIV kalibriert ist.
Eingang X5 ("EXTERN")	BNC-Buchse: Eingang für externes Trigger- oder Horizontalablenkungssignal. Eingang für Trigger-Qualifiziersignal.

2.2.2.5. Übrige

CAL	Testpunkt an der eine Rechteckspannung von ≈ 2 kHz und eine Amplitude von 1,2 $V_{S\text{-}S}$ ± 1 % zur Verfügung steht. Für Tastkopfkompensation und/oder Prüfung der Vertikalablenkgenauigkeit.
Externe Speisung	Eingangsbuchse an der Rückwand des Geräts gestattet Betrieb mit einer externen Gleichspannung. Speise-Nennspannung 23 V bis 27 V, Stromaufnahme ≈ 2 A.
Netzspannungsumschalter	Ist vor dem Anschluss an das örtliche Netz, den in Abschnitt 2.1.2. gegebenen Angaben entsprechend, einzustellen.

2.2.3. Elektronenstrahlröhre und POWER Einstellelemente

ILLUM AND POWER ON	Stufenlose Einstellung der Rasterbeleuchtung; zugleich Netzschalter. Signallampe zeigt den Ein-Zustand (ON) an.
INTENS	Stufenlose Einstellung der Bildhelligkeit.
FOCUS	Stufenlose Einstellung zur Fokussierung des Elektronenstrahls.
TRACE ROTATION	Schraubendrehereinstellung zur Ausrichtung der Schreibspur mit den horizontalen Rasterlinien.

2.3. BEDIENUNGSANLEITUNG

2.3.1. Einschalten des Geräts

Vor Anschluss des Geräts an eine Stromquelle sind die in Abschnitt 2.1. gegebenen Anleitungen genauestens auszuführen. Das Gerät wird normalerweise nach einer Anwärmzeit von etwa 15 Minuten den Spezifikationen (siehe Abschnitt 1.2.) entsprechen. Wenn das Gerät jedoch grosser Kälte ausgesetzt war (z.B. unter Frostbedingungen nachts im Auto gelassen) und danach in einen warmen Raum gebracht wird, ist eine Anwärmzeit von etwa einer halben Stunde einzuhalten (siehe Abschnitt 1.2.4.).

2.3.2. Vorbereitendes Verfahren

Mit diesem Verfahren lässt sich feststellen ob das Gerät ordnungsgemäss funktioniert und es ergibt einen tauglichen Ausgangspunkt für den Beginn von Messungen.
Siehe Abb. 2.2. bezüglich der Lage der Bedienungselemente.
Bringe die Einsteller INTENS und FOCUS in Mittelstellung.
Beide Drucktasten "0" eindrücken.
Taste AUTO drücken und mit Schalter TIME/DIV einen durchschnittlichen Zeitkoeffizienten zwischen 10 µs/div und 10 ms/div wählen.
Mit allen übrigen Drucktasten in Normalstand (nicht gedrückt) lassen sich die Schreibstrahlspuren von Kanal A und Kanal B mit den entsprechenden Einstellern POSITION auf dem Bildschirm darstellen.
Mit Bedienungselement INTENS eine mittlere Bildhelligkeit und mit FOCUS eine gute Strahlfokussierung einstellung.

2.3.3. POWER ON test

Bei Einschaltung löst der Mikroprozessor ein Testprogramm zur Prüfung der unmittelbaren Nachbarschaft des Mikroprozessors aus.
Wenn dieser Test einen Fehler ergibt, so bleibt die Elektronenstrahlröhre dunkel.
Wenn nur das RAM einen Fehler enthält dann wird die fehlerhafte Adresse binär dargestellt.

2.3.4. Service Test

Das Gerät enthält ein Testprogramm zur Lokalisierung eines möglichen Funktionsfehlers.
Dieses Programm wird durch gleichzeitiges Eindrücken der Tasten STORE TRIG und STORE REF gewählt.
Das Testprogramm besteht aus einer Anzahl der Reihe nach aktivierter gesonderter Testmoduln. Der erste Modul wird eingegeben, wenn das Testprogramm gewählt wird.
Ein Testmodul behandelt ein bestimmtes Testverfahren oder die Prüfung eines bestimmten Teils der Schaltung.
Um zum nächsten Testmodul überzugehen, muss Taste START/STOP eingedrückt und losgelassen werden.
Gleichzeitiges Drücken der "STORE REF" und "0" Tasten führt wieder zum Operationsprogramm zurück.
Nähere Einzelheiten über den "Service Test" sind im "SERVICE MANUAL" dieses Geräts enthalten.

2.4. LOGIC STATE ANALYZER BETRIEB

Mit dem PM 3540 in dieser Betriebsart kann der Anwender die Software-Programmbefehle so überprüfen, wie sie bei der Entwicklung in das System eingegeben wurden:

- Die Darstellung binär, oktal oder hexadezimal erfolgen, angepasst an die jeweilige individuelle Anwendung.
- Die Darstellung von 16 seriellen Bits in bis zu 16 parallelen Kanälen (d.h. das dargestellte Fenster) kann über den gesamten gespeicherten Datenblock von 64 x 16 Bits geschoben werden (paging oder durchblättern).
- Der erfasste Datenblock kann, relativ zu einem vorgewählten Wort (das Triggerwort), im Datenstrom aufwärts und abwärts verschoben werden.
- Ein Referenzblock von Daten kann mit einem zweiten Block von erfassten Daten verglichen werden. Auf diese Weise lässt sich ein möglicher Fehler auf rasche und einfache Weise auffinden.
- Das Gerät kann für Triggerung auf den Fehler selbst oder in der Nähe des Fehlers, eingestellt werden. Alle diese Einrichtungen ermöglichen dem Anwender eine eingehende und zweckmässige Analyse jedes anfallenden digitalen Problems.

2.4.1. Datenerfassung

Datenerfassung ist jener. Vorgang bei welchem digitale Signale abgetastet und in binäre Form umgesetzt werden. Bezüglich Umsetzung in Binärform siehe Abschnitte "Schwelle" (2.4.2.).
Die Daten die dargestellt werden sollen, müssen über die entsprechenden PM 8820 Tastköpfe (Technische Daten, siehe Abschnitt 3) und die Eingänge an der rechten Seite des Geräts (X15, X16 und X17) angeschlossen werden.
Es ist zu beachten, dass nicht benutzte Eingänge automatisch Nullpegelsignale ergeben (siehe auch Abschnitt 2.5.4. Kanal löschen).

2.4.2. Schwellwerte

Um eine einwandfreie Datenerfassung zu erlangen muss der logische Binärzustand der einlaufenden Daten in einwandfreie binäre Impulse umgesetzt werden. Zu diesem Zweck ist richtige Einstellung der Schwellenspannung erforderlich. Dies geschieht für den TTL-Pegel automatisch; zusätzlich ist eine variable Schwelle eingebaut (ADJ).
Zur Einstellung des Schwellenwertes in ADJ-Betrieb, verbinde ein Voltmeter mit Testpunkt MEAS und stelle das entsprechende Potentiometer ein (Schraubendrehereinstellung).
Es ist zu beachten, dass der Schwellenwert nur bei Anwendung der Tastköpfe PM 8820 gilt und dass der Schwellenwert nicht unabhängig für die Eingänge X15 (Kanäle niedrigster Ordnung) X16 (Kanäle höchster Ordnung) und X17 (Takt und Qualifizier) gewählt werden kann.

2.4.3. Takt

Der Takt ist ein wiederholtes Signal, dass die Abtastfrequenz für die zu messenden Eingangssignale festlegt. Bei jedem Taktimpuls wird ein "sample" (Abtastung) der Eingangssignale erfasst und im Eingangsspeicher des PM 3540 gespeichert.
Obiger Vorgang wird von der START-Funktion ausgelöst und von der STOP-Funktion dieser Taste beendet. Dieses Taktsignal wird von einem, im zu prüfenden Gerät vorhanden Takt oder anderem Signal, abgeleitet. Man spricht von einem Synchrontakt, weil der Abtastvorgang des Analysators mit dem zu prüfenden Gerät synchron läuft. Als Taktvorgang kann die positive oder negative Flanke des Gerättakts gewählt werden.

2.4.4. Taktqualifizierer

Eine selektivere Datenerfassung ist möglich, indem der Takt mit einer zusätzlichen Bedingung (Taktqualifizierer) kombiniert wird.
Der Taktqualifizierer kann "1", "0" oder "X" (don't care) abgeschaltet sein, einstellbar mit Hilfe der Wahltasten 1, 0 oder X.

2.4.5. Triggerung (siehe Abschnitt 1.2. für die technischen Daten)

Der Triggervorgang stoppt die Datenerfassung und Speicherung, der Eingangsspeicher enthält nur jene Daten die vor Empfang des Triggersignals erfasst wurden.
Die Speicherinhalt steht zur Darstellung zur Verfügung.
(PUNKT 2.4.5. gilt nur wenn TRIGGER DELAY nicht gedrückt ist.)
Als Triggerquelle kann gewählt werden:

- Ein bestimmtes vorgewähltes Triggerwort, welches im Datenstrom vorkommt (d.h. interne Triggerung)
- Ein extern angelegtes Signal.
- Manuell.

2.4.5.1. Interne Triggerung

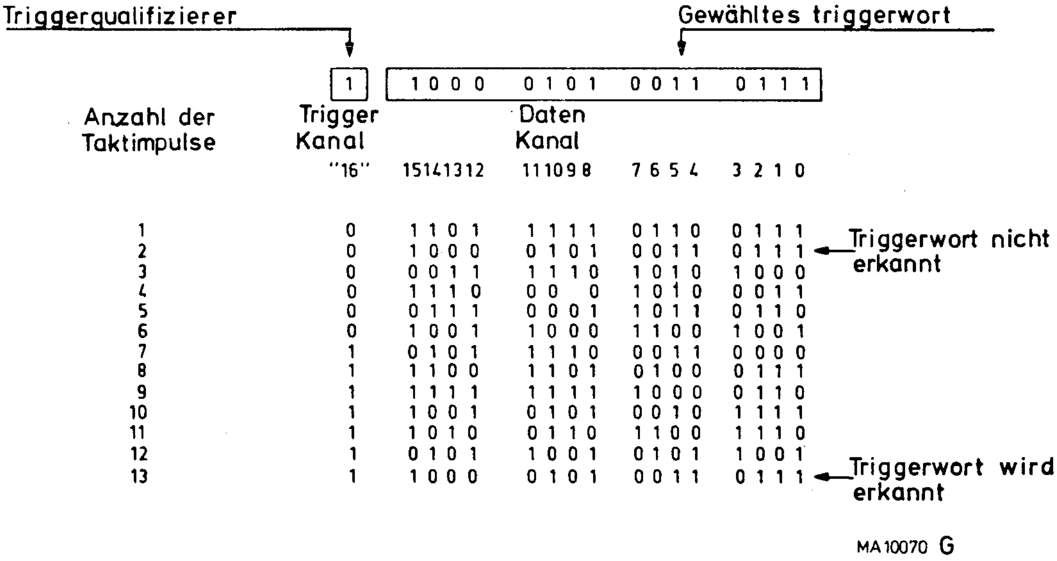
Triggerung erfolgt wenn der Analysator eine Übereinstimmung zwischen einem Wort im Datenstrom und einem bestimmten vorgewählten Triggerwort erkennt.
Dieses Triggerwort besteht aus einer Kombination von logischen "1" und "0", die mit Hilfe der Wahltasten (siehe 2.5.2.) **oder** aus der Darstellung mit Hilfe der Taste "STORE TRIG" gewählt werden können.
Für Eingangskanäle, die nicht verwendet werden oder deren Bit-Information unwichtig ist muss die X-Funktion (don't care) gewählt werden.
Interne Triggerung lässt sich mit Triggerverzögerung und Triggerqualifizierer kombinieren.

2.4.5.2. Externe Triggerung

Triggerung erfolgt auf ein an die BNC-Buchse "EXTERNAL" auf der Frontplatte gelegtes Signal. Triggerung findet nur statt, wenn der Triggereingang an der gewählten Taktflanke freigegeben ("wahr") ist und das Triggerwort nur "don't care's" (x ... x) enthält, d.h. abgeschaltet ist.
Externe Triggerung lässt sich mit Triggerverzögerung kombinieren und ist in der Betriebsart QUAL wirksam.

2.4.5.3. Manuelle Triggerung

Triggerung findet durch Drücken der Taste START/STOP statt, wenn die Information "NOT TRIGGERED" angezeigt wird. Die manuelle Triggerung ist allen übrigen Triggerbedingungen übergeordnet (auch der Triggerverzögerung) und ermöglicht das Sichtbarmachen des Speicher-Inhalts, selbst wenn das Triggerwort unbekannt oder unauffindbar ist.



Anzahl der Taktimpulse	Trigger Kanal "16"	Daten Kanal 15 14 13 12	11 10 9 8	7 6 5 4	3 2 1 0
	1	1 0 0 0	0 1 0 1	0 0 1 1	0 1 1 1
1	0	1 1 0 1	1 1 1 1	0 1 1 0	0 1 1 1
2	0	1 0 0 0	0 1 0 1	0 0 1 1	0 1 1 1
3	0	0 0 1 1	1 1 1 0	1 0 1 0	1 0 0 0
4	0	1 1 1 0	0 0 0	1 0 1 0	0 0 1 1
5	0	0 1 1 1	0 0 0 1	1 0 1 1	0 1 1 0
6	0	1 0 0 1	1 0 0 0	1 1 0 0	1 0 0 1
7	1	0 1 0 1	1 1 1 0	0 0 1 1	0 0 0 0
8	1	1 1 0 0	1 1 0 1	0 1 0 0	0 1 1 1
9	1	1 1 1 1	1 1 1 1	1 0 0 0	0 1 1 0
10	1	1 0 0 1	0 1 0 1	0 0 1 0	1 1 1 1
11	1	1 0 1 0	0 1 1 0	1 1 0 0	1 1 1 0
12	1	0 1 0 1	1 0 0 1	0 1 0 1	1 0 0 1
13	1	1 0 0 0	0 1 0 1	0 0 1 1	0 1 1 1

Abb. 2.3. Triggerwort und Trigger Qualifier

2.4.6. Triggerqualifizierer

Der Triggerqualifizierer ist als zusätzliche Bedingung für das gewählte interne Triggerwort vorgesehen. Das Triggerqualifizierersignal wird über die BNC-Buchse "EXTERNAL" auf der Frontplatte angeschlossen und ist in Betriebsart "QUAL" wirksam.
Eine selektivere Datenerfassung ist möglich, indem das Triggersignal mit einer zusätzlichen Bedingung (Triggerqualifizierer) kombiniert wird. Der Triggerqualifizierer kann als ein 17 Kanal zur Triggererkennung betrachtet werden (siehe Abb. 2.3.).
Dieser Eingang wird bei Eingangspegel "hoch" als "wahr" bewertet (für die technischen Daten, siehe Abschnitt 1.2.1.5.). Durch Anschluss des Triggertastkopf PM 8810 an die BNC-Buchse "EXTERNAL" lässt sich die Triggerwahlkapazität erweitern.

2.4.7. Triggerverzögerung

Durch Eindrücken der Taste DELAY wird die Triggerverzögerung eingeschaltet. Die Triggerverzögerung ist eine Anzahl von Taktimpulsen, die zwischen dem Erscheinen des Triggerwortes oder des externen Triggersignal und dem tatsächlichen Zeitpunkt der Triggerung verstreichen. Das bedeutet, dass der zu messenden Datenblock abwärts im Datenstrom positioniert werden kann (siehe Abb. 2.4.).

Nach Triggerung (Post-Triggering)

Durch Anwendung der Triggerverzögerung (TRIGGER DELAY) kann faktisch jeder beliebige Datenblock zeitlich nach einem eingestellten Triggerwort (oder Triggersignal) gewählt werden.
Die Triggerverzögerung ist zwischen 0 und 9999 Taktimpulsen einstellbar und wird den Textzeilen angegeben. Wenn beispielsweise die Triggerverzögerung auf 63 gestellt ist, dann wird der gesamte Speicher mit Daten gefüllt, welche direkt hinter dem Triggerwort (oder Triggersignal) erschienen sind (siehe Abb. 2.4.).

Vor Triggerung (Pre-Triggering)

Wenn die Triggerverzögerung ausgeschaltet wird (Taste DELAY-rücksetzen) oder wenn sie auf 0 gestellt wird, so erfolgt die Triggerung im gleichen Augenblick in dem das Triggerwort an den Dateneingängen vorhanden ist. In diesem Fall enthält der Speicher 63 Worte, die unmittelbar vor dem Triggerwort (oder Triggersignal) erfasst wurden (siehe Abb. 2.4.).

Mittel-Triggerung (Centre-Triggering)

Bei dieser Triggerung wird das Triggerwort in die Mitte des erfassten Datenblocks gebracht.
Hierzu muss eine Triggerverzögerung von 32 Taktimpulsen gewählt werden (siehe Abb. 2.5.).

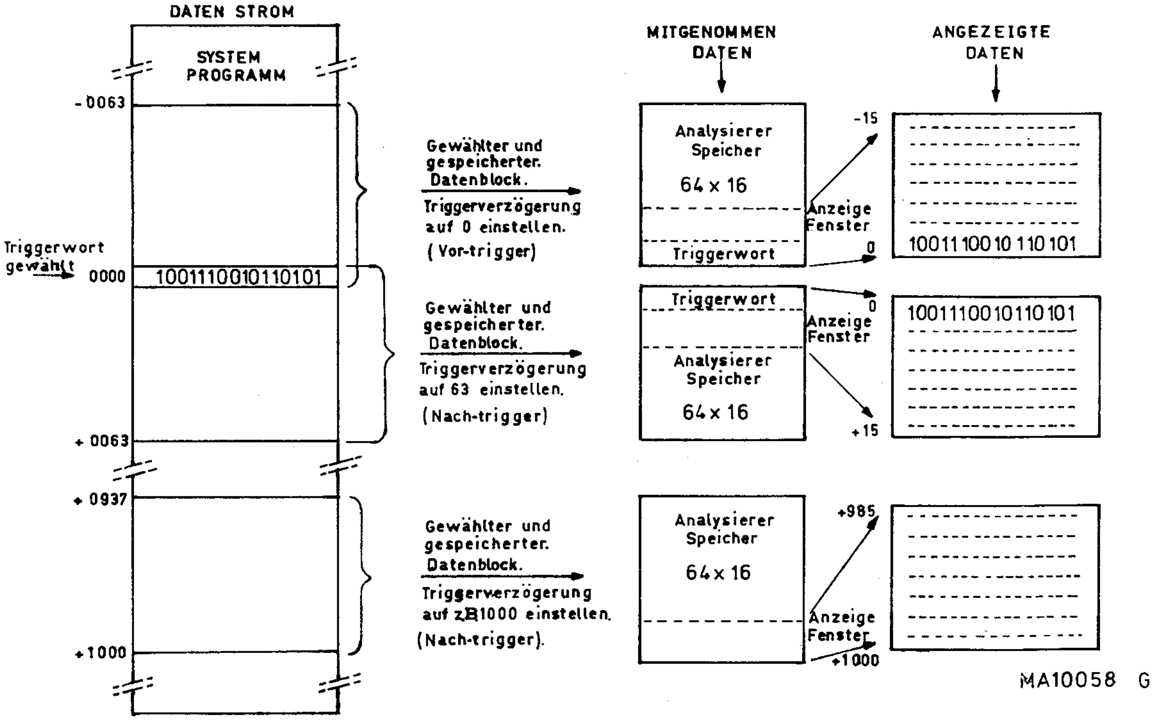

DATEN STROM
SYSTEM PROGRAMM
-0063
Triggerwort gewählt
0000
1001110010110101
+0063
+0937
+1000
Gewählter und gespeicherter. Datenblock.
Triggerverzögerung auf 0 einstellen.
(Vor-trigger)
Gewählter und gespeicherter. Datenblock.
Triggerverzögerung auf 63 einstellen.
(Nach-trigger)
Gewählter und gespeicherter. Datenblock.
Triggerverzögerung auf z.B.1000 einstellen.
(Nach-trigger).
MITGENOMMEN DATEN
Analysierer Speicher
64 x 16
Triggerwort
-15
Anzeige Fenster
0
+15
+985
+1000
ANGEZEIGTE DATEN
1001110010110101
MA10058 G

Abb. 2.4. Darstellung zwischen Triggerverzögerung, Speicher und Zusammenhang

2.4.8. **Darstellung** (Abb. 2.5.)

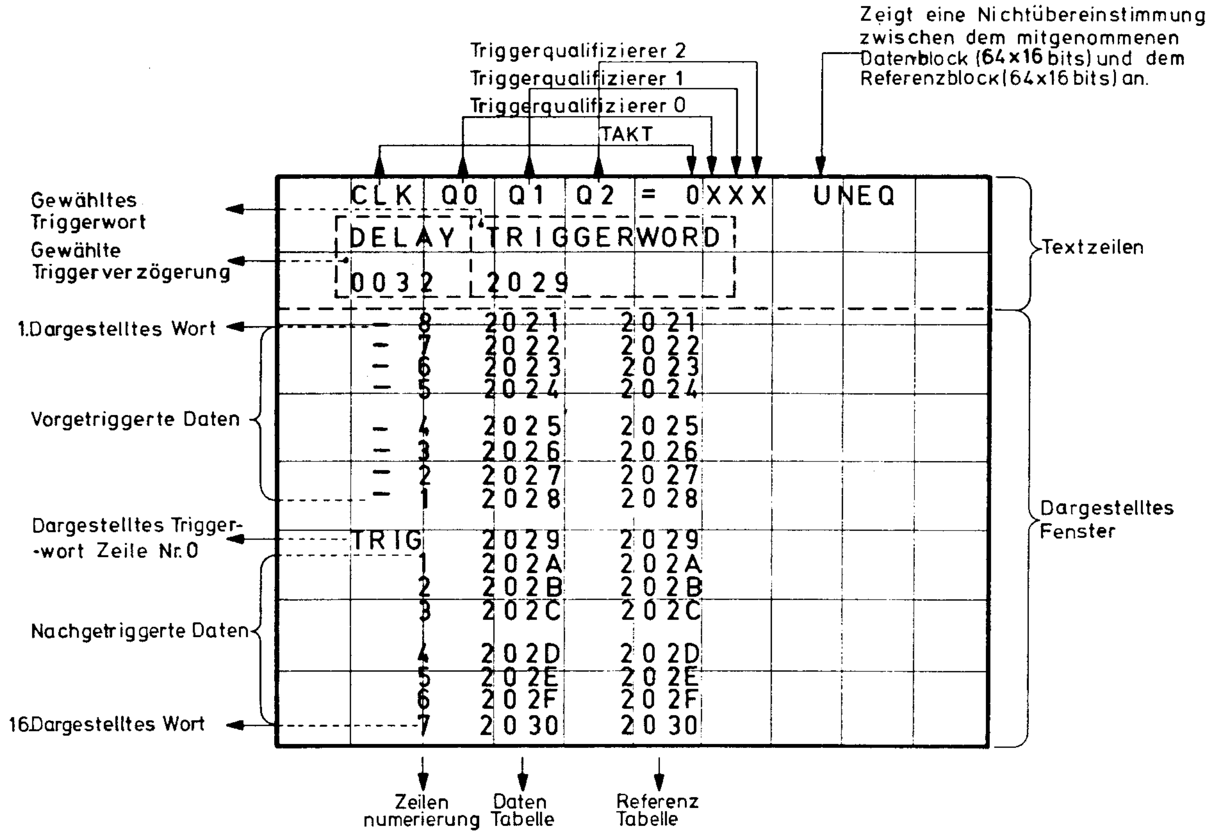
Im Analysatorbetrieb wird auf der Elektronenstrahlröhre des Oszilloskops in Tabellen-Format dargestellt. Die Daten können binär, oktal oder hexadezimal sedezimal dargestellt werden.

Die im oberen Bildschirmteil kontinuierlich dargestellten Textzeilen enthalten Angaben über Parameter und Zustand des Geräts. Die Zeilennummern sind Speicheradressen und auf das erfasste Triggerwort bezogen, so dass die Position der dargestellten Details (d.h. Anzeigefenster) innerhalb des gespeicherten Blocks zu jeder Zeit bekannt ist.

2.4.8.1. Paging (Bildschirmblättern)

Wie in Abb. 2.5. veranschaulicht, ist die tatsächliche Darstellung auf dem Bildschirm (d.h. das Fenster) ein 16-Wort Ausschnitt aus dem gesamten gespeicherten Datenblock.

Damit der Rest des gespeicherten Datenblocks dargestellt werden kann, wird die "Roll" Funktion der Cursorsteuerung angewandt, mit ihrer Hilfe lässt sich der gesamte 64-Wort Datenblock, in Teilbereichen dargestellt, überprüfen (paging).



Zeigt eine Nichtübereinstimmung zwischen dem mitgenommenen Datenblock (64x16 bits) und dem Referenzblock (64x16 bits) an.
Triggerqualifizierer 2
Triggerqualifizierer 1
Triggerqualifizierer 0
TAKT
CLK Q0 Q1 Q2 = 0XXX UNEQ
DELAY TRIGGERWORD
0032 2029
Gewähltes Triggerwort
Gewählte Triggerverzögerung
Textzeilen
1.Dargestelltes Wort
Vorgetriggerte Daten
Dargestelltes Trigger-wort Zeile Nr. 0
Nachgetriggerte Daten
16.Dargestelltes Wort
Dargestelltes Fenster
- 8 2021 2021
- 7 2022 2022
- 6 2023 2023
- 5 2024 2024
- 4 2025 2025
- 3 2026 2026
- 2 2027 2027
- 1 2028 2028
TRIG 2029 2029
1 202A 202A
2 202B 202B
3 202C 202C
4 202D 202D
5 202E 202E
6 202F 202F
7 2030 2030
Zeilen numerierung
Daten Tabelle
Referenz Tabelle

MA 10071 G

Abb. 2.5. Darstellung

2.5. WAHL DER LOGIK ANALYSATOR BETRIEBSART

Durch eindrücken der Taste LSA/OSC wird der Analysatorbetrieb gewählt. Die Eingangssignale die dargestellt werden sollen, werden an einer ansteigenden oder abfallenden Taktflanke (dies auf den gewählten Schwellwert bezogenen) im Speicher festgehalten. Das Speicherformat ist 64 x 16 Bit Worte.

2.5.1. Parameterwahl

Mit eingedrückter Taste SELECT befindet sich das Gerät in der Auswahlbetriebsart. Bevor eine Logikanalyse vorgenommen werden kann, muss das Triggerwort, Taktflanke, Taktqualifizierer und möglicherweise auch Triggerverzögerung eingestellt werden.
Zu diesem Zweck lassen sich die Parameter mit Hilfe des horizontalen CURSOR Einstellers, des vertikalen CURSOR Einstellers, des vertikalen CURSOR Einstellers und der Wahltasten 1/+, X (don't care) und 0/– spezifizieren. Diese Wahltasten sind sowohl schriftweise wie auch kontinuierlich anwendbar. Die Datenerfassung wird ausgelöst, wenn die Taste START oder die Taste AUTO eingedrückt ist.
(Nur wirksam wenn Taste SELECT ausgerastet ist.)

2.5.2. Wahltasten

Die Wahltasten ermöglichen dem Anwender die Spezifizierung der Parameter in den Textzeilen und haben unterschiedliche Funktionen, abhängig von den verschieden Parametern und von der Darstellungsart.

"1, +" : Drucktaste mit automatischer Auslösung

Funktion "1"	: logische Eins für	– Triggerwort in BIN Format – Triggerqualifizierer und Taktflanke	
Funktion "+"	: Addierfunktion für	– Verzögerung in 0-9 Folge – Triggerwort im Falle von	 HEX Format in 0...F Folge OCT Format in 0...7 Folge

"X" : Drucktaste mit automatischer Auslösung

Funktion "X"	: (don't care") ohne Einfluss für	– Triggerwort in BIN Format – Triggerqualifizierer

"0, –" : Drucktaste mit automatischer Auslösung

Funktion "0"	: logische Null für	– Triggerwort in BIN Format – Triggerqualifizierer und Taktflanke	
Funktion "–"	: Subtrahierfunktion	– Verzögerung in 9-0 Folge – Triggerwort im Falle von	 HEX Format in F...0 Folge OCT Format in 7...0 Folge

2.5.3. Cursor und CURSOR Einstellelemente

Im Auswahlbetrieb (d.h. mit eingedrückter SELECT Taste) ist der Cursor durch ein aufgehelltes Digit in den Textzeilen gekennzeichnet.
Der Cursor wird mit Hilfe der CURSOR-Schalter in horizontaler oder vertikaler Richtung verschoben.

2.5.4. Einsteller BLANK und ROLL

Wenn sich das Gerät nicht im Auswahlbetrieb befindet (d.h. mit ausgerasteter Taste SELECT) dann wird der vertikale (CURSOR) Einsteller als Rollfunktion benutzt und ermöglicht so "Bildschirmblättern" (Paging), durch den gesamten 64-Wort Speicher.
Der horizontale (CURSOR) Einsteller dient zur Kanalunterdrückung.
In der Tabellendarstellung werden die Kanäle (Spalten) von links (d.h. Kanal 15) nach rechts (Kanal 0) unterdrückt, siehe hierzu Abb. 2.6.
Rückruf erfolgt durch Betätigung des horizontalen (CURSOR) Einstellers in entgegengesetzter Richtung.

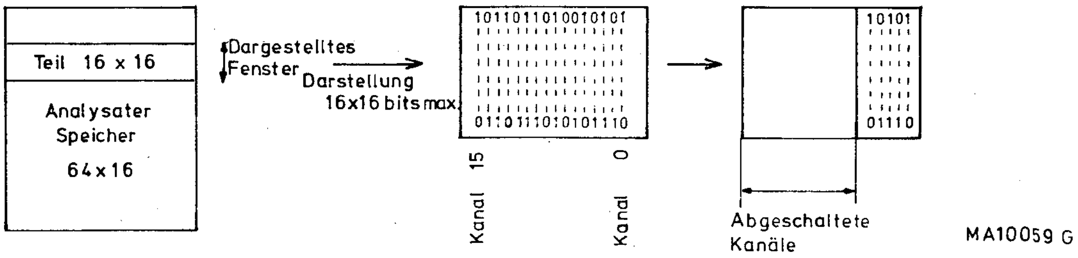


Abb. 2.6. Dargestelltes Fenster und Kanalabschaltung

2.5.5. Triggerwort-Einstellung

Nach Eindrücken der SELECT-Taste erscheint der Cursor in den Textzeilen. Die Stellung des Cursors muss mit Hilfe der horizontalen oder der vertikalen Cursor-Einstellelemente auf die einzustellende Stelle im Triggerwort verschoben werden. Wenn ein Triggerwort binär dargestellt wird, muss der Cursor auf eines der 16 Digits gesetzt werden.

Ein "1", "0" oder "X" (nicht bewertet) Logikzustand wird über die Drucktasten 1/+, X und 0/— gewählt.

Der Cursor springt automatisch zur nächsten Digitposition. Bei Oktal- oder Hexadezimalanzeige muss der horizontale CURSOR Einsteller betätigt werden, nachdem über Drucktasten 1/+, X oder 0/— eingestellt worden ist.

Mit Hilfe von Taste "+" wird die gewünschte 0...7 oder 0...F Einstellung erreicht. Mit Taste "—" dementsprechend die Reihenfolge 7...0 oder F...0.

2.5.6. Wahl von Taktflanke und Taktqualifizierer

Nach Eindrücken der SELECT-Taste und nachdem der Cursor auf in die linke obere Stelle d.h. die Taktposition des Bildschirms gebracht ist, lässt sich über die Tasten 1/+ und 0/— die ansteigende Flanke "1" oder die abfallende Flanke "0" des Taktsignals wählen.

Die nächsten drei Stellen auf die der Cursor gebracht wird, können zur Spezifizierung des Taktqualifizierers benutzt werden. Das heisst, Daten werden nur erfasst wenn bis zu drei zusätzliche Logikkonditionen erfüllt werden. Das geschieht durch die Wahl von einer "1", "0" oder "X" Bedingung für jeden Taktqualifizierer-Eingang.

Anmerkung: Wenn kein Taktqualifizierer angeschlossen ist, dann wird der entsprechende Eingang mit dem Pegel "0" bewertet.

2.5.7. Drucktaste START/STOP

Dies ist eine Druck-Taste mit zwei Funktionen:

- Der erste Tastendruck ist der Startbefehl.
  Durch den Startbefehl wird der Zeitpunkt bestimmt zu welchem der Analysator die Erfassung und die Speicherung der Daten beginnt.
- Der zweite Tastendruck stoppt die Erfassung der Daten.
  Die START/STOP Taste kann in Betriebsart AUTO (automatisch) und SINGLE (einzel) betrieben werden (siehe Abb. 2.7. und 2.8.).

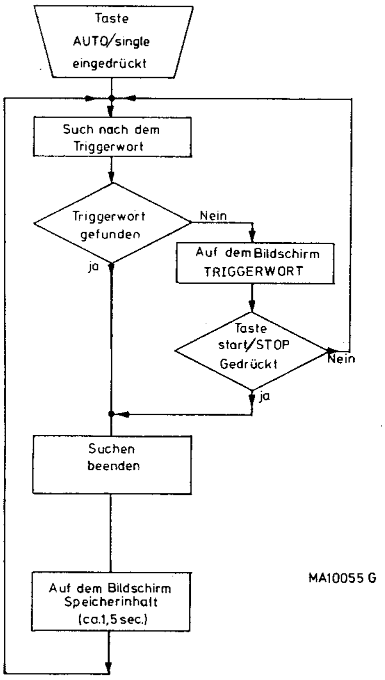

Taste AUTO/single eingedrückt
Such nach dem Triggerwort
Triggerwort gefunden
Nein
ja
Auf dem Bildschirm TRIGGERWORT
Taste start/STOP Gedrückt
Nein
ja
Suchen beenden
Auf dem Bildschirm Speicherinhalt (ca.1,5 sec.)
MA10055 G

Abb. 2.7. START/STOP Funktion bei Betriebsart AUTO

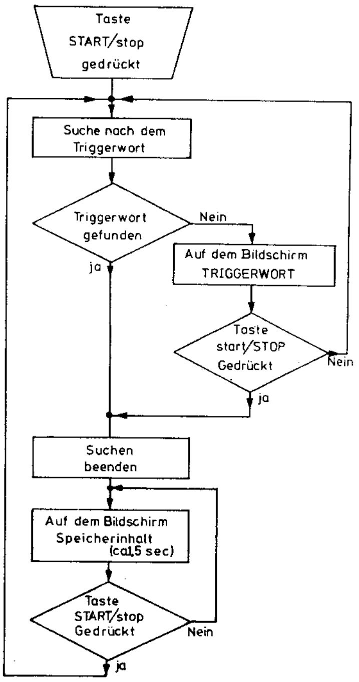

Taste START/stop gedrückt
Suche nach dem Triggerwort
Triggerwort gefunden
Nein
ja
Auf dem Bildschirm TRIGGERWORT
Taste start/STOP Gedrückt
Nein
ja
Suchen beenden
Auf dem Bildschirm Speicherinhalt (ca1,5 sec)
Taste START/stop Gedrückt
Nein
ja

Abb. 2.8. START/STOP Funktion bei Betriebsart SINGLE

2.5.8. AUTO/SINGLE Betriebsart

Daten können auf zweierlei Weise erfasst werden:

- AUTOmatische wiederholte Abtastung
- SINGLE (Einzel-) Abtastung über START von Hand.

Im "AUTO" Betrieb (Taste gedrückt) erfolgt die Abtastung der Daten jede Sekunde, resultierend in einer kontinuierlichen Erneuerung des Speicherinhalts und folglich der dargestellten Wahrheitstabellen.
Automatische Abtastung wird gestoppt sobald AUTO/SINGLE auf SINGLE gestellt wird (siehe Flussdiagram Abb. 2.7. START/STOP Vorgang bei Betriebsart AUTO).
Diese Methode eignet sich besonders für die Beobachtung sich wiederholender Abläufe da sich individuelle Bitänderungen leicht ermitteln lassen.
Bei Betriebsart SINGLE (Taste ausgerastet) beginnt die Datenerfassung bei einer START Betätigung, und wird gestoppt wenn das gewählte Triggerwort mit einem Datenwort im Datenfluss übereinstimmt, oder aber nach einer STOP Betätigung (siehe Abb. 2.8. START/STOP Vorgang in SINGLE Betrieb). Das bedeutet dass der Speicher Daten, enthält, die in einem einzigen Vorgang erfasst wurden.
Der SINGLE-Betrieb liefert eine kontinuierliche Darstellung des Speicherinhalts. Diese Betriebsart ist besonders zur Analyse eines bestimmten Teils im Datenstrom geeignet.

2.5.9. STORE TRIGgerwort Taste

Die STORE/TRIG Drucktaste ist ein Bedienungselement, welches beim Loslassen der Taste wirksam ist (Drucktaste COMPARE muss ausgerastet sein). Wenn STORE/TRIG betätigt wird, dann wird das erste auf dem Bildschirm dargestellte Wort (einschliesslich der vorhandenen Werte der unterdrückten Kanäle) das "neu" gewählte Triggerwort und wird auch in der Textzeile angezeigt (siehe Abb. 2.5.).
Diese Möglichkeit der Speicherung eines "neuen" Triggerworts kann benutzt werden um eine Fehlerbedingung zu repräsentieren.
Es wird beispielsweise eine Fehlerbedingung im Datenstrom angezeigt. Diese Fehlerbedingung wird mit Hilfe des Schalters "ROLL" in die 1. Wort Position verschoben und danach als ein "neues" Triggerwort gespeichert. Das Gerät wird dann nur beim Auftreten dieses bestimmten Fehlers getriggert.

2.5.9.1. STORE TRIG in Betriebsart AUTO

Diese Betriebsart wird durch Eindrücken der Tasten AUTO und STORE TRIG gewählt. Mit dieser Betriebsweise lässt sich das "paging" über den gespeicherten Datenblock hinaus erweitern. Das bedeutet, dass nach jedem STORE TRIG Vorgang ein neues Triggerwort und somit automatisch ein neuer Datenblock mit neuer Information gewählt wird. Diese Betriebsart lässt sich ebenfalls mit Triggerverzögerung (DELAY) kombinieren.

2.5.10. TRIGGER DELAY Wahl

Nach Eindrücken der Tasten SELECT und DELAY kann, nachdem der Cursor in die Verzögerungsposition gebracht ist, die Auswahl der Verzögerung erfolgen. Der Cursor muss auf eine der vier Digitpositionen gestellt werden, welche dann mit Hilfe von Taste "+" für eine 0...9 Folge eingestellt werden, oder für eine 9...0 Folge mit Hilfe von Taste "–".
Das Triggern des Geräts kann bis um 9999 Taktimpulse verzögert werden.
Durch nochmaliges Drücken von Taste DELAY wird die Triggerverzögerung ausgeschaltet.

2.5.11. COMPARE Betriebsartwahl

Mit eingerasteter COMPARE Taste werden neu erfasste Daten mit zuvor gespeicherten fehlerfreien Daten verglichen. (Siehe Abschnitt 2.5.12. "STORE REFerenz.)
Hierzu wird ein zweiter 64-Wort Speicher zur Speicherung von Referenzdaten verwendet. Der erfasste Datenblock von 64-Worten wird mit dem Referenzdatenblock auf einer Bit für Bit Grundlage verglichen. Jede Nichtübereinstimmung zwischen den beiden Blöcken wird in der Textzeile mit der Information "UNEQ" (ungleich) angegeben und auf dem Bildschirm mit aufgehellten Digit(s) gekennzeichnet.
Im HEX- und im OCT-Betrieb wird sowohl die Eingangsdatentabelle als auch die Referenztabelle dargestellt.
Beim BIN-Betrieb wird nur die Eingangsdatentabelle dargestellt.
Alle fehlerhaften Bits erscheinen aufgehellt z.B. bedeutet eine aufgehellte 0 sollte eine 1 im Referenzspeicher.

Anmerkung: Das Erscheinen von "EQ" oder "UNEQ" in der Textzeile Anzeige bedeutet, dass der letzte Datenblock von 64 x 16 Bits, gleich oder ungleich bezogen auf einen früher gespeicherten Datenblock von 64 x 16 Bits, war.

2.5.11.1. COMPARE in Betriebsart AUTO

Diese Betriebsart wird durch Drücken der Tasten COMPARE und AUTO gewählt. Daten werden automatisch aufgezeichnet und verglichen. Diese Betriebsart erweist sich als sehr nützlich für Daten die nur sporadisch nicht übereinstimmen.
Sobald irgendeine Nichtübereinstimmung zwischen neu aufgezeichneten Daten und Referenzdaten aufgespürt wird, wird die Datenerfassung gestoppt.
Die Nichtübereinstimmung wird durch die Information "UNEQ" und durch ein aufgehelltes Digit in der Darstellung signaliert. Wenn die Nichtübereinstimmung nicht dargestellt wird, so kann sie mit Hilfe des Schalters "ROLL" auf dem Bildschirm sichtbar gemacht werden.
Die Datenerfassung kann durch Betätigung der START-Taste erneut ausgelöst werden.

2.5.12. STORE REFerenz

Das Gerät befindet sich in dieser Betriebsart wenn Taste COMPARE eingedrückt ist und Taste STORE REF betätigt wird. Bereits erfasste Daten werden vom Eingangsspeicher in den Referenzspeicher übertragen. Die beiden Datenblöcke werden auf einer Bit für Bit Grundlage verglichen.

2.6. OSZILLOSKOPBETRIEB

In dieser Betriebsart kann das PM 3540 als Universal-Zweikanal Oszilloskop angewandt werden.
Durch die interaktive Beziehung zwischen Analysator und Oszilloskop wird Triggerung beider Teile des Geräts vom gleichen vorgewählten Triggerwort ermöglicht.

2.7. WAHL DES OSZILLOSKOPBETRIEBS

Mit der Drucktaste LSA/OSC in ausgerastetem Zustand ist der Oszilloskopbetrieb gewählt und somit sämtliche Einstellelemente und Buchsen des Oszilloskopteiles des PM 3540 einsatzbereit.

2.7.1. Eingangskopplung (AC/DC, 0)

AC-Kopplung (Drucktaste eingedrückt) dient zum Sperren der Gleichspannungskomponente eines Signals.
Die AC-Einstellung unterdrückt die Niederfrequenzen, wodurch sinusförmige Signale niedriger Frequenz abgeschwächt und Rechtecksignale niedriger Folgefrequenz verformt werden. Der Abschwächungsgrad wird von der Eingangs RC-Zeitkonstanten (0,1 s) bestimmt.
Die Eingangs RC-Zeitkonstante wird um den Faktor 10 erhöht, wenn 10 : 1 passive Tastköpfe verwendet werden.
Wenn auf AC-Kopplung geschaltet wird dauert es etwa fünf Eingangs RC-Zeiten bevor der Strahl auf den Mittelwert des Eingangssignals stabilisiert ist.
AC-Positions Messungen können nicht gegenüber Erde vorgenommen werden.

0-Stellung: Die Verbindung von Eingangsschaltung und Eingangsbuchse wird aufgetrennt und die Eingangsschaltung kurzgeschlossen um die 0-Stellung zu überprüfen.

DC-Kopplung (Gleichspannungskopplung) (Drucktaste ausgerastet) ermöglicht Messungen über den gesamten Frequenzbereich, bis hinab auf Gleichspannung.

2.7.2. Anwendung von Tastköpfen (siehe auch Abschnitt 3.1. "Einzelheiten betreffend Zubehör)

1:1 passive Tastköpfe sollten nur für Gleichspannung und Niederfrequenzen eingesetzt werden.
Die kapazitive Belastung schwächt hohe Frequenzen ab oder erhöht die Anstiegszeit von Messsignalen (abhängig von der Quellimpedanz).

10:1 passive Tastköpfe besitzen eine kleine kapazitive Belastung; gewöhnlich etwa 10 pF bis 20 pF.
FET-Tastköpfe sind besser, besonders wenn Messungen von Messpunkten mit hoher Impedanz vorgenommen oder an der oberen Frequenzgrenze des Logik-Skops ausgeführt werden sollen.

10:1 passive Tastköpfe müssen vor Gebrauch ordnungsgemäss kompensiert werden. Ungenaue Kompensation hat Impulsverformung oder Amplitudenfehler bei hohen Frequenzen zur Folge.
Für genaue Einstellung kann der CAL-Testpunkt verwendet werden (siehe Abb. 2.9.).

2.7.3. Einstellen der Abschwächer-Tastköpfe

- Den Tastkopf mit der Y_A oder Y_B Eingangsbuchse verbinden und die Tastkopfspitze an Testpunkt CAL legen.
- Mit einem kleinen Schraubenzieher durch die Bohrung in der Kompensationsdose den Trimmer einstellen, um ein einwandfreies Bild zu erhalten (siehe Abb. 2.9.).

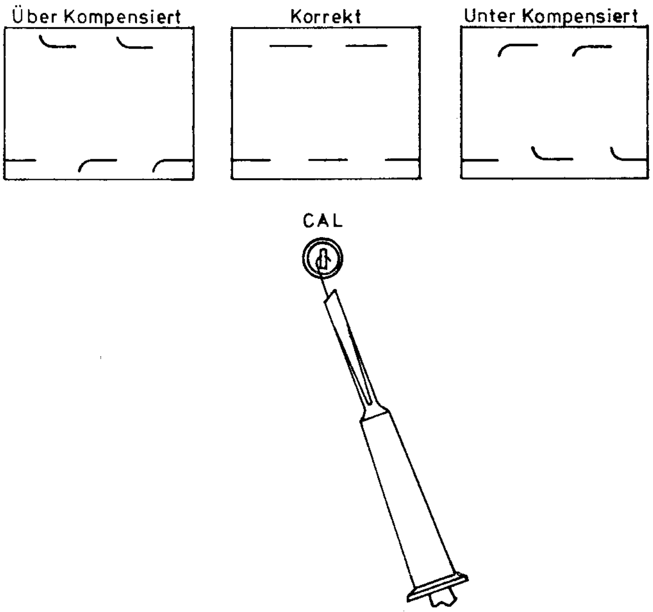


Abb. 2.9. Abgleich eines Abschwächer Tastkopfs **MA9820 G**

2.7.4. Auswahl der gechoppten oder der alternierenden Darstellungsarten

(A, ALT, CHOP, ADD, B)

Im Zweikanalbetrieb (CHOP oder ALT eingedrückt), muss für relativ lange Ablenkzeiten (von .1 ms/div bis .5 ms/div) oder bei vorkommender niedriger Ablenk-Folgefrequenz, selbst bei kurzen Ablenkzeiten, die Darstellungsart CHOP verwendet werden. (CHOP eingedrückt.)
Stellung ALT würde unter diesem Umständen Vergleiche zwischen Signalformen erschweren, weil die beiden Signale nacheinander dargestellt werden.
Wenn die Darstellung jedoch schnell genug ist, um von der Chopperfrequenz unterbrochen zu werden, muss die alternierende Darstellung gewählt werden (ALT eindrücken), gewöhnlich bei Ablenkzeiten schneller als .1 ms/div.

2.7.5. Differenz Betriebsart

Betriebsart A minus B lässt sich durch Drücken von ADD und Ziehen des Knopfes POSITION von Kanal B einstellen. Bei Messungen bei denen Signalleitungen bedeutende Gleichtaktsignale führen (z.B. Brumm) hebt die Differenz-Betriebsart diese Signale auf und lässt den Rest, der von Bedeutung ist, übrig.
Die Fähigkeit des Logik-Skops für die Unterdrückung von Gleichtaktsignalen, ist im CMR-Faktor gegeben (siehe Abb. 2.10).
Um den spezifizierten Grad der Gleichtaktunterdrückung zu erlangen, müssen erst die Kanal A und B Verstärkungen ausgeglichen werden. Dies wird durch Anschluss beider Kanäle an der CAL-Ausgang und durch Einstellung eines der stufenlosen Einstellelemente in dem Schalter AMPL/DIV auf Minimum Ablenkung auf dem Bildschirm erreicht.
Bei Verwendung von passiven 10:1 Messköpfen ist ein ähnliches Ausgleichsverfahren zu empfehlen und zusätzlich durch die Kompensationseinstellung eine Minimum-Ablenkung zu erreichen.

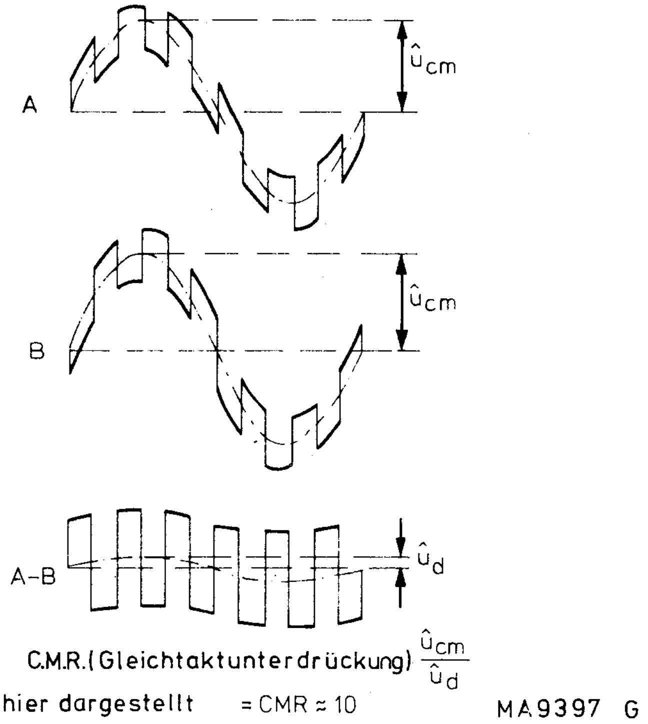

A
ûcm
B
ûcm
A-B
ûd
C.M.R.(Gleichtaktunterdrückung) ûcm/ûd
Wie hier dargestellt = CMR ≈ 10
MA9397 G

Abb. 2.10. Gleichtaktunterdrückung

2.7.6. Wahl der Triggerquelle

Die Triggerquelle wird mit den Frontplatte-Drucktasten TRIG or X DEFL eingestellt (S16).

A B EXT DATA
└COMP┘ └QUAL┘

- **Interne Triggerung** ist die im allgemeinen meist angewandte, da sie nur ein Signal erfordert (das Y_A oder Y_B Eingangssignal) um stabile Triggerung zu erlangen.
- **Externe Triggerung.** Falls mehrere Signale abgetastet werden, ist es günstig ein externes Signal zur Triggerung zu benutzen. Bei einer Anderung des Eingangssignals ist Einstellung und Neueinstellung der Trigger-Bedienungselemente (LEVEL, SLOPE und SOURCE) nicht nötig. Ausserdem bleiben die beiden Eingänge Y_A und Y_B für Untersuchungen der Signalformen verfügbar.
- **Wahl der Triggerquelle.** Beim Vergleich synchroner Signalformen mit ungleicher Folgefrequenz immer das Signal mit der niedrigsten Folgefrequenz als Triggersignal wählen. Wenn nicht, könnten Doppelbilder (gechopped) oder falsche Zeitverschiebungen (alternierend) entstehen.
- **Zusammengesetzte (composite) Triggerung.** Bei interner Triggerung werden Triggersignale von entweder dem A-Kanal, den B-Kanal Vorverstärkerstufen oder wenn COMP durch Eindrücken der beiden Tasten A und B gewählt werde von der Verzögerungsleitungs-Treiberstufe, die dem elektronischen Kanalschalter folgt, erhalten.

  Zusammengesetzte Triggerung bietet drei Vorteile:
  1. In der Differenz Betriebsart (A-B Messungen) wird die Triggerung wird nicht von Gleichtaktsignalen gestört.
  2. Für Einkanal-Betrieb ist es nicht nötig Triggerquellen von A nach B oder umgekehrt zu schalten.
  3. In alternierender Betriebsart lassen sich Signale vergleichen, die nicht in zeitlicher Beziehung stehen.

Anmerkung: Bei Anwendung zusammengesetzter Triggerung in Zweikanalbetrieb (alternierend) und wenn dabei nur ein Signal angelegt ist (an Eingang A oder B), ist stabile Triggerung nicht erlangbar. Das ist nicht ungewöhnlich, da die Triggerquelle auch von A nach B geschaltet wird (siehe Abb. 2.11). Bei Anwendung zusammengesetzter Triggerung in (gechopptem) Zweikanalbetrieb ist stabile Triggerung nicht möglich, weil das System von den Umschalt-Spitzen der Choppersignale getriggert wird.

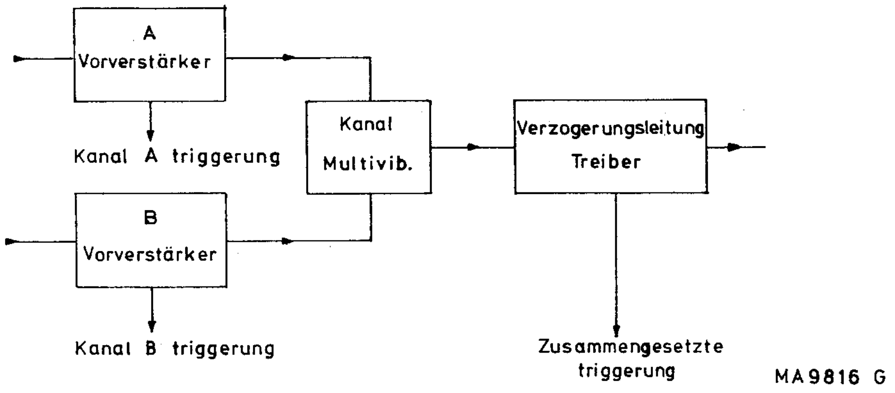


Abb. 2.11. Blockschaltbild der Triggerschaltung "COMPOSITE"

- **Daten-Triggerung.** Durch Einstellung des Triggerwortes auf einen bestimmten bekannten Logikzustand, der unmittelbar vor dem Auftreten eines Fehlers im Datenstrom erfolgt, kann die Oszilloskop-Zeitbasis getriggert werden, so dass das Gerät nur das Echtzeitverhalten zweier gewählter Signale (angeschlossen über Y_A und Y_B) nach dem bestimmten Logikzustand darstellt.
  Damit dies erreicht wird muss man den bestimmten Logikzustand als Triggerwort einstellen und mit gedrückter Taste DATA in Oszilloskopbetrieb arbeiten.
  Nun lässt sich das detaillierte zeitabhängige Verhalten von zwei beliebig gewählten Signalen im gleichen Augenblick, in dem der ermittelte Fehler vorkommt, betrachten.
- **Qualifizierte Triggerung.** Wenn sowohl Taste DATA als auch EXT eingedrückt ist, kann man die Triggerung nur dann erfolgen lassen wenn zusätzlich ein "hoher" Logikpegel am Trigger-Qualifizierer-Eingang anliegt. Ein nicht angeschlossener Trigger-Qualifizier Eingang gilt als dauernd "hoch".

  Bemerkung: Bei Messungen in DATA oder QUALifizier Betriebsart sind die Stellungen DC und "+" Flanke des Triggerwahlschalters S2 anzuwenden (siehe Abb. 2.2.).

2.7.7. Einstellen der Triggerbetriebsart

(AUTO, AC, DC, TV, +/–)

Betriebsart AUTO ist äusserst nützlich, da dabei das Bild stets sichtbar ist, auch wenn keine Triggersignale vorhanden sind. Ausserdem bewirkt diese Betriebsart für eine Signalamplitude die grösser ist als ein Teil (div.) eine stabile Triggerung unabhängig von der Stellung des Pegeleinstellers LEVEL; der Einstell-Bereich wird automatisch auf den Spitze-Spitzewert des für Triggerung gewählten Signals eingestellt.
Auf diese Weise wird die LEVEL-Einstellung bei kleinen Amplituden des Triggersignals erleichtert.
Die Betriebsart AUTO lässt sich für Signale mit niedriger Folgefrequenz (10 Hz oder niedriger) nicht verwenden, weil dies freilaufende Ablenkung zwischen Triggerimpulsen ermöglichen würde. Deshalb ist bei Signalen niedriger Folgefrequenz die normale Triggerung anzuwenden (AC oder DC gedrückt).
Bei normaler Triggerung wird die Zeitablenkung nur dann ausgelöst wenn ein Triggersignal angelegt wird und LEVEL entsprechend eingestellt ist.
Mit gedrücktem AC oder DC ist der Bereich des Einstellers LEVEL festgesetzt (+ oder – 8 Teile (div) oder mehr in den äussersten Stellungen des LEVELPotentiometers, bezogen auf die Bildschirmmitte).
Die Gleichspannungskomponente des Triggersignals lässt sich durch Eindrücken von AC sperren.
Dies ist nützlich wenn durch ein Wechselspannungsignal, dass einem hohen Gleichspannungspegel überlagert ist, getriggert werden soll. Bei AC-Kopplung verändert sich der Pegel bei welchem die Darstellung beginnt mit der Änderungen des Mittelwertes des Triggersignals. Der Triggerpegel ist nicht auf Signalerde bezogen. Dies kann bei Signalformen die im Zeitabstand von Zyklus zu Zyklus varieren Instabilität zur Folge haben.
Normalerweise ist Anwendung der DC-Stellung vorzuziehen. Flankenwahl ist mit Drucktaste +/– vorzunehmen.
Bei Betriebsart TV ist für negative Videosignale "–" einzustellen und "+" für positive Videosignale. Einsteller LEVEL ist bei Betriebsart TV nicht wirksam. Eine zusätzliche Betriebsart ist vorhanden wenn keine Tasten eingedrückt sind, eine Zeitablenklinie ist auf dem Bildschirm sichtbar, wenn kein Triggersignal vorhanden ist, während der Pegelbereich des Einstellers LEVEL fest ist.

2.7.8. Dehnung der Zeitablenkung

Die Dehnung wird durch Ziehen des an den Steller X POSITION gekoppelten X MAGN bewirkt. Mit diesem Schalter in Stellung x10 wird die Zeitablenkgeschwindigkeit 10-fach vergrössert. Die Ablenkzeit wird daher durch Teilung des angezeigten Wertes TIME/DIV durch 10 bestimmt.

2.7.9. XY Messungen

Für XY Messungen steht der Schalter TIME/DIV auf X DEFL, die Quelle der Horizontalablenkung wird mit Drucktaste EXT X DEFL oder TRIG (S16) eingestellt.
XY Messungen ergeben ein zweckmässige Mittel für Frequenz- oder Phasenverschiebungsvergleiche durch Darstellung mit Lissajous Figuren. Messungen bis zu 100 kHz sind möglich wobei der Phasenfehler zwischen den Oszillografenkanälen geringer als 3° ist.
Nachstehende Tabelle zeigt die Empfindlichkeit der verschiedenen XY-Betriebsarten.

X DEFL	EMPFINDLICHKEIT
A	AMPL/DIV A ± 10 %
B	AMPL/DIV B ± 10 %
EXT	0,5 V/DIV
DATA	Für diese Betriebsart nicht anwendbar

2.8. VERFAHREN ZUM ENTFERNEN VON SICHERUNGEN, BILDRÖHRENRAHMEN UND KONTRASTPLATTE

2.8.1. Abnehmen der Abdeckhauben

Es ist immer darauf zu achten, dass vor Abnahme irgendwelcher Deckel oder Platten das Gerät vom Netz getrennt ist.
Das Gerät ist durch drei Abdeckhauben geschützt: eine Frontschutzhaube, ein Mantel mit Tragbügel und eine Abdeckplatte für die Rückwand.
Die Frontschutzhaube muss erst angebracht werden, dies erleichert Abnahme des Mantels und der Rückwandplatte.
Den Abnehmen geschieht wie folgt:

- Den Tragbügel von der Frontplatte wegschenken, zu diesem Zweck die beiden Drehzapfenknöpfe drücken (Abb. 2.12).
- Das Gerät auf seiner Frontschutzhaube auf eine ebene Fläche stellen.
- Die beiden Schlitzschrauben auf der rückwärtigen Abdeckplatte lösen.
- Die rückwärtige Abdeckplatte abheben und den Stecker aus der Netzteil-Leiterplatte ziehen.
- Den Gehäusemantel abnehmen.
- Die Frontplatte wird zugänglich, wenn das Gerät horizontal aufgestellt wird und die Frontschutzhaube abgezogen wird.

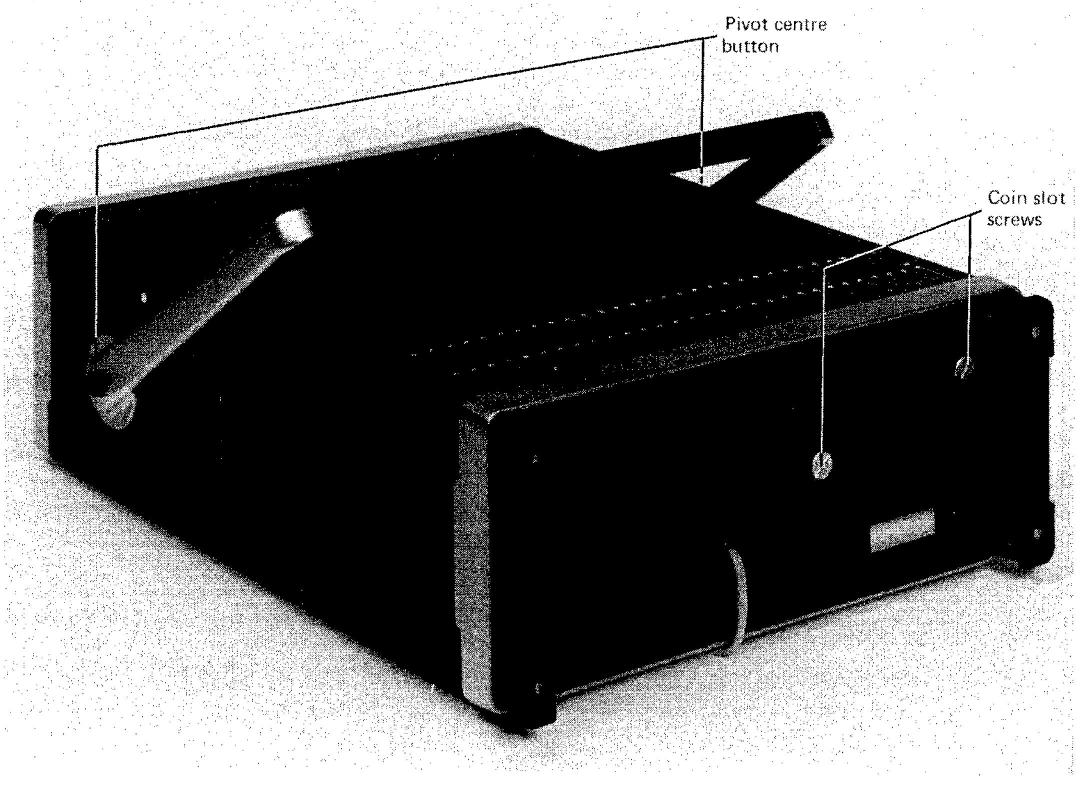


Abb. 2.12. Abnehmen der Abdeckhauben

2.8.2. Ausbau des Netztransformators

- Gehäusemantel und Rückwand abnehmen (Abschnitt 2.8.1.).
- Nach Lösung der 4 Kreuzschlitzschrauben den Deckel des Spannungsadapterfachs abnehmen.
- Die vier Kreuzschlitzschrauben, mit denen der Deckel des Transformatorfachs befestigt ist, lösen.
- Den Deckel mit dem daran befestigten Transformator abheben und gleichzeitig den Draht zwischen Transformator und Spannungsadapter aus dem Schlitz im Transformatorfach schieben.
- Transformator und Übertemperatursicherung sind nun zugänglich und können ersetzt werden.

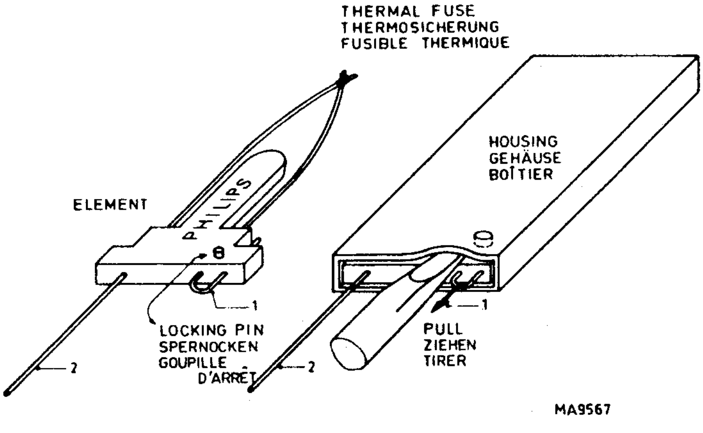

THERMAL FUSE
THERMOSICHERUNG
FUSIBLE THERMIQUE
HOUSING
GEHÄUSE
BOÎTIER
ELEMENT
PHILIPS
θ
1
LOCKING PIN
SPERNOCKEN
GOUPILLE D'ARRÊT
2
2
1
PULL
ZIEHEN
TIRER
MA9567

Abb. 2.13. Ersetzen der Übertemperatursicherung

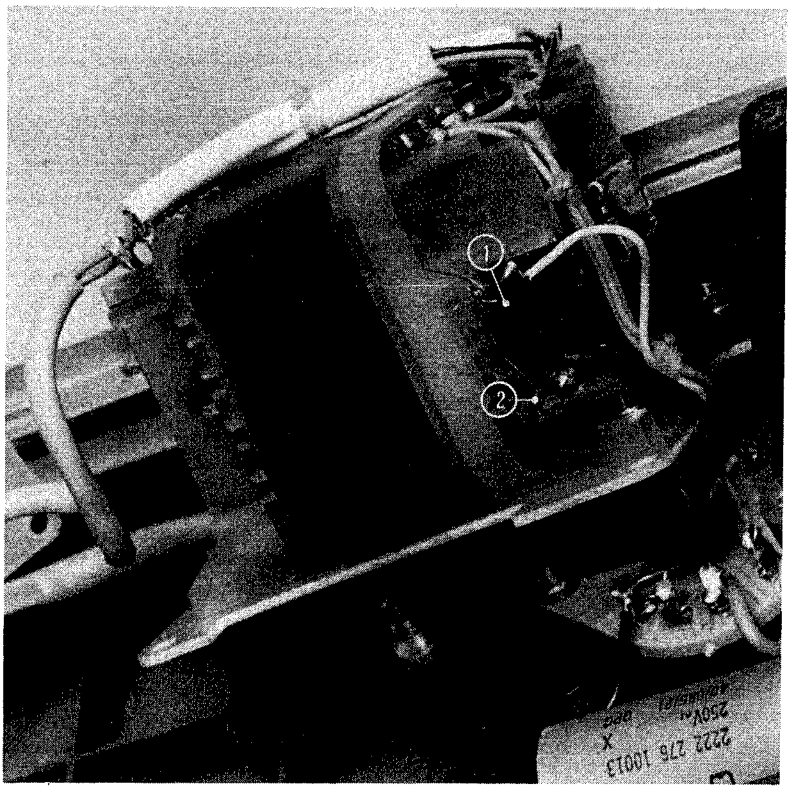


Abb. 2.14. Ersetzen der Übertemperatursicherung

2.8.3. Ersetzen der Übertemperatursicherung F101

- Netztransformator entfernen (Abschnitt 2.8.2.).
- Sicherungsanschlussdrähte 1 und 2 ablöten (Abb. 2.13 und 2.14).
- Es wird nur der Sicherungsdraht der alten Sicherung ersetzt und nicht die gesamte Sicherung; zu diesem Zweck das Gehäuse der Sicherung etwas nach aussen biegen, die Sperrnocken freilegen und den Draht herausziehen.
- Die neue Sicherung nehmen und den Sicherungsdraht auf die gleiche Weise wie oben beschrieben aus seinem Gehäuse ziehen.
- Den neuen Sicherungsdraht in das Gehäuse der alten Sicherung stecken bis die Sperrnocken im Loch einschnappen. Die Schleife im Sicherungsdraht muss nach Anschluss 1 gerichtet sein.
- Die Sicherungsdrähte und Anschlüsse 1 und 2 löten.

2.8.4. Ersetzen der Sicherung F201

- Gerätemantel und Rückwand abnehmen (Abschnitt 2.8.1.).
- Die sich auf der Netzteil-Leiterplatte befindliche Sicherung F201 ist nun Zugänglich und kann ersetzt werden.

2.8.5. Abnehmen des Bildröhrenrahmens und der Kontrastplatte

- Den Bildröhrenrahmen an den unteren Ecken festhalten und vorsichtig von der Frontplatte ziehen (Abb. 2.15).
- Die Kontrastplatte kann nun gehutsam aus dem Rahmen gedrückt werden.

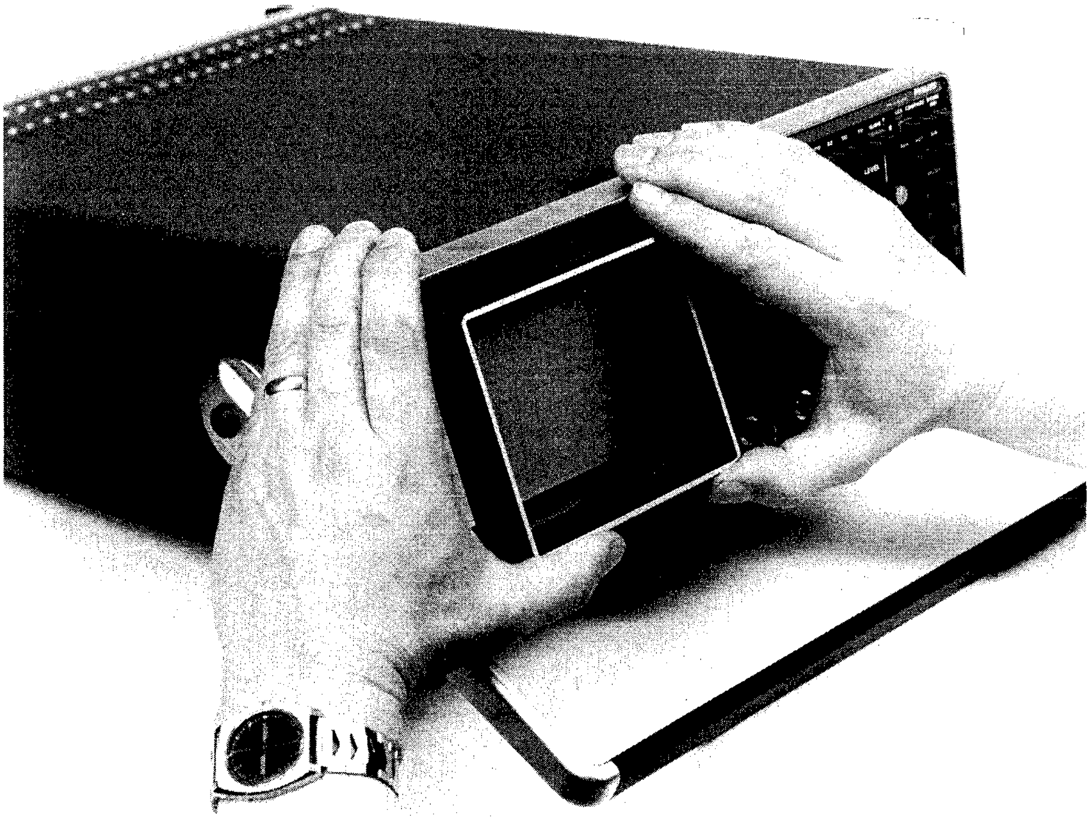


Abb. 2.15. Abnehmen des Bildröhrenrahmens und der Kontrastplatte

2.9. WARTUNG

Das Gerät erfordert im allgemeinen geringfügige Wartung, da es keine Bauteile enthält die dem Verschliess ausgesetzt sind. Um jedoch verlässlichen und einwandfreien Betrieb zu gewährleisten, ist das Gerät gegen Feuchtigkeit, Hitze, Korrosion erzeugende Einflüss oder übermässigen Staub zu schützen. Das Aussehen der mit Nextel-Lack überzogenen Manteloberfläche kann sich nach einiger Zeit verschlechtern. Zur Reinigung einen weichen Putzlappen mit Ethanol oder einem gewöhnlichen Haushaltswaschmittel verwenden. Scheuernde Lappen oder Reinigungsmittel dürfen nicht benutzt werden, da sie die Oberfläche zerkratzen.

WARNUNG: Der Nextel-Lack ist Ethanolbeständig jedoch nicht gegen Alkohol oder methylierten Alkohol (Brennspiritus) der die Oberfläche angreift (durch eine der denaturierenden Substanzen).

Zum Reinigen der Frontplatte und Rückwand, sowie des Kontrastfilters der Elektronenstrahlröhre keine Lösungsmittel wie Trichloräthylen oder Azeton verwenden.
Einen weichen Lappen, Tuch oder Watte mit Wasser und gewöhnlichem Haushaltwaschmittel, etwas Alkohol oder Brennspiritus verwenden.
Prüfen ob nach längerem Gebrauch die Öffnungen im Gehäusemantel nicht mit Staub verstopft sind. Falls erforderlich der Gehäusemantel entfernen und die Öffnungen mit Druckluft freiblasen.

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3.1. DESCRIPTION OF THE BLOCK DIAGRAM

3.1.1. Analyzer main sections

3.1.1.1. The main sections (as indication in the block diagram Fig. 3.1) of the analyzer part are:

- Data aquisition circuit, with 16 identical input channels, each with a 64 bit deep memory.
  At each clock pulse, a sample of the data present at the input is written into the (data input) memory.
  As long as the clock is active, data is written into the memory thus overwriting former data.
- Qualifier and clock circuit
  One of the functions of this block is to stop the clock signal as soon as the trigger condition is valid.
  The content of the data input memory is then stable and can be displayed.
- Display circuit
  This circuit includes a.o. digital to analog convertors and a character generator.
  The circuit enables the various display modes to be displayed on the screen of the c.r.t.
- Micro-processor system
  This circuit controls the various circuits of the instrument, and consists of a high-speed microprocessor (8085) with ROM, RAM and Decoder circuits to generate control signals.

3.1.1.2. The main working principle

There are two main operational modes:

1. *Memory content display mode*
   This is in principle a stationary situation which is initiated when all trigger conditions are valid.
   This situation remains as long as no start function is present.
2. *Data aquisition mode.*
   As soon as a start function is present the instrument starts capturing data and puts this data into the data input memory.
   Data is captured at the selected clock edges.
   At each captured data word, the instrument checks whether the trigger is valid.
   As soon as the trigger is valid, data intake stops, and the memory content is displayed.
   Generally the trigger condition consists of:
   Comparison of the data word which is in the input circuit of the instrument, with the preselected trigger word, and checking whether the trigger delay is zero.
   As long as the trigger delay is not zero, the trigger delay number is decremented at each captured data word.
   The display shows "not trigger" as long as:
   – the preselected trigger word is not found - or
   – the preselected trigger delay not zero.

   Note that in this situation the instrument does not react on most of the front panel switches. Only the manual trigger function (i.e. operating the STOP knob) puts the instrument in the display mode.

3.1.2. Oscilloscope main sections

The main sections (see Fig. 3.1.) of the oscilloscope part are:

3.1.2.1. Y Channel

The vertical channels A and B for the signals to be displayed are identical, each comprising an input coupling switch, an input step attenuator, an impedance converter and a preamplifier with trigger pick-off.
A channel multivibrator, controlled by the display mode pushbuttons, switches either channel A or channel B to the final Y amplifier via the delay line. The channel multivibrator is operated by a pulse at the end of the sweep, and offers an uninterrupted display of the A and B waveforms in the ALT mode. In the CHOP mode the multivibrator is free-running and provides a chopped display of the two signals. In the ADD position, both switching amplifiers are connecting the signals through thus adding channels A and B. By inverting the B channel amplifier (PULL TO INVERT B) the A-B mode is obtained.

The AMPL/DIV switches provide x1 or x10 gain control of the preamplifier, which offers in conjunction with the step attenuator a full range of deflection coefficients in a 1-2-5 sequence.

3.1.2.2. Triggering

To initiate sweeps, trigger signals can be derived from the A and B vertical channel preamplifiers, from an external source, or internally from the trigger circuit in the analyzer part as selected by the trigger source switch. With A and B pushbuttons both depressed, composite triggering is derived from the delay-line driver stage. The polarity of the trigger signal, negative or positive-going, on which the display will start is determined by changing the output polarity of the impedance convertor.

With the AUTO switch depressed, the peak-to-peak level detector comes into operation. The peak-to-peak level of the signal then determines the range of the LEVEL control.

With AC or DC depressed, the range of the LEVEL control is fixed.

In the TV mode the LEVEL control is inoperative and the TV sync separator is switched onto circuit, thus initiating sweeps with line or frame pulses as dictated by the setting of the TIME/DIV switch.

3.1.2.3. Time-base circuit

For normal internal time-base operation the horizontal amplifier is fed by sweeps from the time-base circuit.

With AUTO depressed, in the absence of trigger signals, the output of the sweep generator is fed back via the hold-off circuit and gate to its input. This causes sweeps to free-run and a resultant trace is displayed on the screen. As soon as the AUTO control circuit detects a trigger (i.e. change in the output of the sweep-gating logic) the sweep is fed back to the sweep-gating logic. This causes the circuit to revert to thenormal triggering mode in which sweeps are initiated only by trigger pulses at the input of the sweep-gating logic.

With AC or DC depressed, AUTO control is made inoperative. Sweeps are then only produced provided a trigger signal is present and the LEVEL control appropriately set.
The display can be magnified in the horizontal direction by increasing the gain of the final amplifier.

In the EXT position of the TIME/DIV switch, the sweep generator output to the final amplifier is inhibited and the impedance convertor is connected directly to the final amplifier. In this way, the signals normally selected for triggering, or an external source, can now be used for horizontal deflection.

3.1.2.4. Hold-off circuit

The hold-off stage, as its name implies, "holds-off" triggers from the input of the time-base circuit until the trace has completely returned and the time-base circuits are completely reset.

3.1.2.5. Z-Axis

The Z amplifier provides for the blanking of the trace during the fly-back and hold-off time. In addition, it blanks the sweep in the CHOP mode during the switching transients. Moreover the trace can be blanked by a signal applied to the external Z-mod input.
The l.f. components of the blanking signal are modulated and demodulated before they are applied to the Wehnelt cylinder together with the a.c. coupled h.f. components.

3.1.2.6. Power supply

The mains (line) supply is transformed and rectified before being applied to a d.c. to a.c. converter.
When the instrument is operated from a battery supply the battery output is connected directly to the d.c. to a.c. converter.
The output of the converter is coupled to a transformer and rectifier which, after rectification, provides the −1.5 kV e.h.t. potential and the circuit supply voltages. The −1.5 kV is also multiplied to 8.5 kV to supply the required total accelerating voltage of ≈ 10 kV.

3.2. DESCRIPTION OF THE CIRCUITS

3.2.1. Circuit description of the analyzer part

General

The philosophy of design is based on integrated circuits and communication bus controlled by a microprocessor system.
Input data is captured by special 8 bit logic probe pods.
A simplified functional flow diagram is given including the interconnection with the oscilloscope part, see Fig. 3.1.

The logic state analyzer section of the PM 3540 LOGIC SCOPE is composed of 3 main sections:

- *Data Aquisition (Fig. 3.1. the part "data aquisition circuit" 2, Fig. 3.4.6.)*
  To capture binary data synchronously from the system under test. This is achieved with the 3 special input probes and hardware in integrated circuit form as outlined in paras 3.2.2.1. to 3.2.2.3.
- *Micro processor system (Fig. 3.1., Fig. 3.2. & Fig. 3.4.7.)*
  To process and transfer the captured data in the desired form to the output circuit (i.e. character generation) and to control the communication between all the circuits. This is achieved with the hardware described in paras 3.2.3.1. to 3.2.3.6. and the software contained within the EPROM (D2064).
- *Character generation (Fig. 3.1., Fig. 3.4. & Fig. 3.48)*
  To translate microprocessor outputs to appropriate signals for CRT display in alpha-numeric characters. This circuit is described in paras 3.2.4.1. to 3.2.4.6.

3.2.2. Data Aquisition

Data Aquisition circuit comprises 3 main elements:
- The data path (para 3.2.2.1.)
- Clock and Qualifier circuit (para 3.2.2.2.)
- Triggercircuit (para 3.2.2.3.)

3.2.2.1. The Data path

The description of the data path is in the sequence of the captured data signal flow.

- Data input port's D2006 & D2007
  Two each of 74LS244 act as 8 bit input devices to compensate for the loading of the 9-bit logic pods.
  Both ports are controlled by the control signal WRAM in order to achieve that the data of the system under test can be cut off from the data aquisition system (the port outputs are "three stated"). The parts are used for loading the data input latches (D2012 and D2013) and the trigger-word RAM's (D2009 and D2011). There is one port for the least significant byte of the captured data and one for the most significant byte.
- Data input latches D2012 & D2013
  The two times 74LS374 (8 bit 3-state D-latches) retain the data from the input ports, clocked by the positive going edge of the signal SYSCLK (which is the system clock). Latching the input data is necessary to ensure that the data is stable during writing it into the Data Input Memory.
- Data Input Memory D2018 & D2019
  The Data Input Memory consists of 2 times 82S09 RAM memory, each of 64 x 9 bit configuration, which accept data from the data input latches. On the positive going edge of SYSCLK signal, data is latched in the data input latches and on the negative going edge of SYSCLK the data is written into the Data Input Memory. D2018 contains the least significant byte of captured data and D2019 the most significant. The data stored during the write cycle is read by μProcessor (via multiplexer circuit) under control of the control signal RDIM (Read Data Input Memory).
  The outputs of the two D.I.M.'s are (wired) OR-ed and during the read cycle, only one of the D.I.M.'s can be read at anyone time. Identification of which D.I.M. is being read is by RDIM and either A8 (LSB D.I.M.) or A9 (MSB D.I.M.).
- Address counter D2014 and D2017
  The address counter consists of two 74LS191 binary counters which are cascaded by connecting the "terminal count" output pin 12 of D2014 (via converter gate D2016 pins 4, 5 and 6) to the enable input of counter D2017 to perform a 64 count.
  During the data acquisition cycle (i.e. the write cycle) it acts as an up counter, clocked by the positive going edge of the SYSCLK signal.

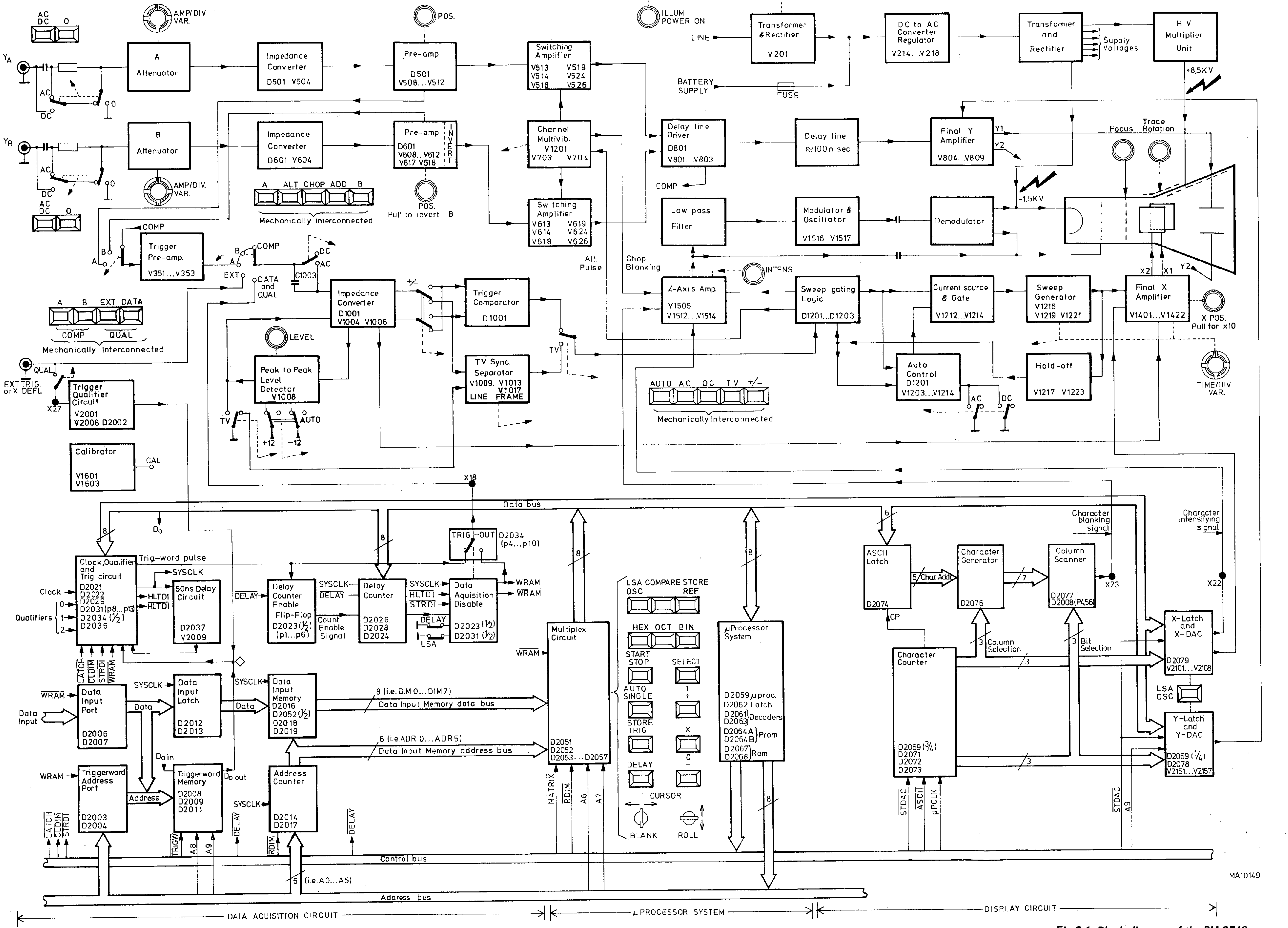

AC DC 0
AMP/DIV VAR.
Y_A
A Attenuator
Impedance Converter D501 V504
POS.
Pre-amp D501 V508...V512
Switching Amplifier V513 V519 V514 V524 V518 V526
ILLUM. POWER ON
LINE
Transformer & Rectifier V201
DC to AC Converter Regulator V214...V218
Transformer and Rectifier
Supply Voltages
H V Multiplier Unit
+8,5KV
BATTERY SUPPLY
FUSE
Y_B
B Attenuator
Impedance Converter D601 V604
Pre-amp D601 V608...V612 V617 V618
INVERT
Channel Multivib. V1201 V703 V704
Delay line Driver D801 V801...V803
Delay line ≈100n sec
Final Y Amplifier V804...V809
Y1
Y2
Focus
Trace Rotation
A ALT CHOP ADD B
Mechanically Interconnected
POS. Pull to invert B
COMP
-1,5KV
Switching Amplifier V613 V619 V614 V624 V618 V626
Low pass Filter
Modulator & Oscillator V1516 V1517
Demodulator
Trigger Pre-amp. V351...V353
B A COMP DC AC
EXT
DATA and QUAL
C1003
Alt. Pulse
Chop Blanking
INTENS.
Z-Axis Amp. V1506 V1512...V1514
Sweep gating Logic D1201...D1203
Current source & Gate V1212...V1214
Sweep Generator V1216 V1219 V1221
Final X Amplifier V1401...V1422
X2 X1 Y2
X POS. Pull for x10
A B EXT DATA
COMP QUAL
Mechanically Interconnected
Impedance Converter D1001 V1004 V1006
+/-
Trigger Comparator D1001
LEVEL
TV
Peak to Peak Level Detector V1008
TV Sync. Separator V1009...V1013 V1017 LINE FRAME
AUTO AC DC TV +/-
Mechanically Interconnected
Auto Control D1201 V1203...V1214
AC DC
Hold-off V1217 V1223
TIME/DIV. VAR.
QUAL
EXT TRIG. or X DEFL.
X27
Trigger Qualifier Circuit V2001 V2008 D2002
TV AUTO +12 -12
Calibrator V1601 V1603
CAL
X18
Data bus
D_0
8
TRIG OUT D2034 (p4...p10)
Clock, Qualifier and Trig. circuit D2021 D2022 D2029 D2031(p8...p13) D2034 (½) D2036
Trig-word pulse
SYSCLK
HLTDI
Clock
Qualifiers 0 1 2
50ns Delay Circuit D2037 V2009
DELAY
Delay Counter Enable Flip-Flop D2023(½) (p1...p6)
SYSCLK DELAY
Count Enable Signal
Delay Counter D2026... D2028 D2024
SYSCLK HLTDI STRDI DELAY
LSA
Data Aquisition Disable D2023 (½) D2031 (½)
WRAM
LATCH CLDIM STRDI WRAM
Data Input Port D2006 D2007
Data Input
Data
Data Input Latch D2012 D2013
SYSCLK
Data Input Memory D2016 D2052(½) D2018 D2019
8 (i.e. DIM 0...DIM7) Data Input Memory data bus
6 (i.e. ADR 0...ADR5) Data Input Memory address bus
Multiplex Circuit D2051 D2052 D2053...D2057
MATRIX RDIM A6 A7
LSA COMPARE STORE OSC REF
HEX OCT BIN
START STOP
SELECT
AUTO SINGLE
STORE TRIG
DELAY
CURSOR
BLANK ROLL
µProcessor System D2059 µ proc. D2062 Latch D2061 D2063 Decoders D2064A D2064B Prom D2067 D2068 Ram
Triggerword Address Port D2003 D2004
Address
Do in
Triggerword Memory D2008 D2009 D2011
Do out
Address Counter D2014 D2017
TRIGW A8 A9 DELAY RDIM DELAY
Control bus
6 (i.e. A0...A5)
Address bus
ASCII Latch D2074
6 Char Addr
CP
Character Generator D2076
7
Column Scanner D2077 D2008(P4,5,6)
Character blanking signal
Character intensifying signal
X23 X22
Column Selection
Bit Selection
Character Counter D2069 (¾) D2071 D2072 D2073
X-Latch and X-DAC D2079 V2101...V2108
LSA OSC
Y-Latch and Y-DAC D2069 (¼) D2078 V2151...V2157
STDAC ASCII µPCLK STDAC A9
DATA AQUISITION CIRCUIT
µ PROCESSOR SYSTEM
DISPLAY CIRCUIT
MA10149

Fig.3.1. Block diagram of the PM 3540

The output signals of the address counter are address locations of the Data Input Memory on which data will be written (data will be written into the DIM during the negative going edge of the SYSCLK signal). These output signals are also fed to the μProcessor (via the multiplexer) to store the address on which the last captured data word has been written into the DIM.
With this stored address, the present DELAY value and the operators setting of the display window by the ROLL switch, the μProcessor calculates (under control of the software) that DIM address which contents will be read out first and on which line number this data will be displayed.
During the data read cycle the address counter acts as a latch to retain the calculated address (sent out by the μProcessor via the address bus) from which DIM location the data has to be read. The low state of the control signal RDIM loads the address counter with the calculated address.

– Valid Data bit flip-flop
  This is a D-flip-flop which is clocked by the signal SYSCLK.
  During data acquisition, a logical "1" is latched and output to the Data Input Memory. Each time a captured data word is written into the DIM, the ninth bit is made "1". At the time the D.I.M. is read (due to the control signal RDIM) by the μProcessor this bit points to captured data words which were written into the D.I.M. during the preceeding write cycle. Before the start of each new data acquisition cycle, the 9th bit of all 64 D.I.M. locations is made a logical "0" by means of the control signal CLDIM (clear data input memory).

3.2.2.2. The Clock and Qualifier circuit

The control signal SYSCLK is processed from the input clock signal and possible qualifier signals. The description of the circuits is in the sequence of the signal flow.

– Clock and Qualifier input gate D2021
  The clock and qualifier input signals are gated by a 74S00 NAND gate to guard against false input levels which can cause false clock or qualifier signals. The clock input is edge sensitive, for the positive going edge a logical "1" has to be selected and for the negative going edge a logical "0".
  A qualifier input is level sensitive. For a low level a logical "0" and for a high level a logical "1" has to be selected.
  An unused qualifier input is indicated with a "X" and is made ineffective via the software.

– Selection latch D2022
  The data signals which determine the polarity and the selection of the input clock and qualifiers are signals which must be available at all times during data aquisition.
  Because the data bus contains these data signals only for a few μp clock cycles they have to be latched, for this reason they are stored in the octal D-flip-flop D2022.
  D0 Contains information concerning the clock polarity
  for the positive going edge D0 is loaded with a "1",
  for the negative going edge D0 is loaded with a "0".
  D1 Contains information concerning the control signal HFTDI (halt data input).
  D2 Contains information concerning the polarity of qualifier Q0.
  D3 Contains information whether qualifier Q0 is selected.
  D4 Contains information concerning the polarity of Q1.
  D5 Contains information whether qualifier Q1 is selected.
  D6 Contains information concerning the polarity of Q2.
  D7 Contains information whether qualifier Q2 is selected.
  When a qualifier is selected the relevant bit location is loaded with a "1". When not selected (thus don't cae) the relevant bit location is loaded with a "0".
  The control of the polarity is also performed by the latch D2022.
  When a high ("1") qualifier polarity is selected the relevant bit location is loaded with a "0" and for a low ("0") polarity with a "1".
  Polarity is changed by the switches "1" and "0" via software.

– Polarity D2029
  The polarity of clock and (or) qualifier signals is determined by the 74S86 "Exclusive OR" gate, designed to select either the rising edge or the falling edge of the input clock which will be used as the triggerpulse for generating the system clock (SYSCLK). D2029 also determines the true level of the clock qualifiers being a logical 1 or a logical 0.

– Selection gate D2033
  If a clock qualifier is not desired it can be ignored by making it "X" on the display. The disabling of a qualifier is made in the 74S64 which is a combined AND-NOR gate. A logic "0" on the input of this circuit (comming from latch D2022) overrules the output from the polarity circuit D2029.

In this way a qualifier is switched off.
The circuit also acts as the clock stop circuit. By disabling the generation of system clock pulses (SYSCLK), the data input (capturing) can be stopped. This is achieved by making the selection output (pin 8) a logical 0. This is possible by making "WRAM" (write RAM) a low level on D2031. Starting id achieved after a STRIDI (Start data input) pulse has made the WRAM signal a high level again. Switching the WRAM level is achieved with flip-flop D2023 (pins 8....13).

- Clock generator D2036)
  The data acquisition is completely under control of the signal SYSCLK. This signal is generated in the D-flip-flop D2036 (pin 1....6). The input clock signal clocks the high level from the selection gata (D2033 pin 8), a positive going signal is made at D2036's Q output (i.e. the SYSCLK signal). The negative going signal is made by the pulse shaper via the active low reset input (pin 1) of this D-flip-flop. Generation of the signal SYSCLK is also possible by pulsing the set input (pin 4) of D2036. The purpose of this is to create clock pulses (64x) after a read D.I.M. cycle to clear the D.I.M. for new data input. SYSCLK generation due to the input clock can be stopped by making the selection output (pin 8 of D2033) a logical "0".
- The pulse shaper is a circuit that keeps the SYSCLK signal (i.e. the Q output pin 5 of D2036) for 50 ns at high level, after which the output (D2037-pin 1) resets itself and the SYSCLK signal is again at low level. The pulse shaper is formed by NOR gate D2037, transistor V2009 and RC network R2033, R2023, R2024 and C2008.

3.2.2.3. The Trigger circuit

- Triggerwork address ports D2003 and D2004
  Two each of 74LS244 accept input from the address bus and output to the triggerword RAM's. The ports are used to separate the address bus from the inputs of the triggerword RAM's.
  This is when the Data Input Ports D2006 and D2007 are transparent (i.e. during data acquisition). The control signals for enabling or disabling the ports are WRAM and $\overline{\text{WRAM}}$ signals.
- Triggerword memory D2009 & D2011
  Each of 82S117 accept the address from either the triggerword address ports (during writing into the triggerword RAM's) or the data input ports (during data acquisition).
  The memory location(s) which represents the triggerword are loaded (during write) with a logical "0" by the μProcessor via data line D0.
  During data acquisition the captured words are fed to the address input of the triggerword memory (during this time the captured words are also fed to the Data Input Memory).
  If a captured data word matches the selected triggerword, the previously loaded logical 0 is read from the memory location and output as a logical 1 (inverting output) at the wired (AND) outputs of the RAM's.
  The triggerword memory is written under control of the signal $\overline{\text{TRIGW}}$.
- EXT Trigger Qualifier Circuit D2002, V2001 & V2008
  Another output which is wired (wired as a AND function) with the triggerword memory output is the external triggerqualifier circuit.
  A triggerword can only be found if this qualifier is high.
- Trigger flip-flop ½D2036 (pins 8 to 13)
  The output from the triggerword memory is synchronized by the SYSCLK signal. When finding the triggerword the trigger signal is clocked by SYSCLK and the output of the trigger flip-flop is fed tothe delay counter via the flip-flop D2023 (pins 1....6).
  This circuitry delivers also the control signals WRAM and $\overline{\text{WRAM}}$ plus the signal for triggering the oscilloscope at the captured triggerword. The Q output of the trigger flip-flop is also fed back to the reset input of the trigger flip-flop to achieve an output signal of 50 ns width (this is due to the circuitry formed by transistor V2009).
- Delay count Enable Flip-Flop (½-D2023 pins 1....6)
  When the triggerword is found the delay counter starts to count the selected trigger delay. The enable input of the delay counter is therefore controlled by the enable flip-flop which enables it on receipt of a pulse from the trigger flip-flop (D2036 pins 8....13). It is disabled when the μProcessor loads the delay counter with the signal $\overline{\text{DELAY}}$.

- Delay counter (D2024; D2026; D2037 & D2028)
  The delay counter creates a trigger delay by counting SYSCLK pulses after a triggerword has been found. The trigger delay value is selected via the screen by the user and is loaded into the counter by the μProcessor under control of the signal $\overline{\mathrm{DELAY}}$. Both the most and the least significant byte are loaded first with the same value and next the least significant byte is loaded again with the real value (MSB loading is prevented by A9 "HIGH" at D2008-10 input). The Delay counter is composed of 4x 74LS190 decade counters.

- Zero detection circuit (½-D2031 & ¼D2032)
  After completion of the count of the selected delay the data acquisition input has to be stopped. The zero state of the delay counter is detected by ½-D2031 (74S20 pin 1....6) a 4 input NANDgate. After synchronizing with the falling edge of the SYSCLK signal, this NAND gate output signal is fed to the clock input of Start/Stop flip-flop D2023 (pins 8....13).

- Start/Stop flip-flop ½xD2023
  The zero state of the least significant counter is not detected by the zero detection circuit. To make the stop function faster the zero state of this counter is fed directly to the Start/Stop flip-flop where it is clocked by the output signal of the zero detection circit.
  The output signal of the Start/Stop flip-flop, WRAM (which means write RAM) is fed to the selection circuit (D2033) via the NAND gate D2031 pin 8 to stop the generation of the signal SYSCLK.
  The start/stop is also controlled by the μProcessor by means of the control signals $\overline{\mathrm{STRDI}}$ (start data input) on the reset input and $\overline{\mathrm{HTLDI}}$ (halt data input) on the set input of the Start/Stop flip-flop.
  The signal $\overline{\mathrm{WRAM}}$ is also recognised by the μProcessor (via data selection circuit D2053....D2057) to make it possible to display data when data capture is ready.

- Trig-out D2034, D2032 and D2039
  The oscilloscope can be triggered on recognition of the triggerword (and after a possible trigger delay) by the output signal of the NAND gate D2034 pin 8. This signal comes either from delay counter (WRAM) or straight from the Q output of the trigger flip-flop D2036 pin 9.
  If delay is off and the PM 3540 is in OSC mode the output from the trigger flip-flop D2036 pin 9 triggers the oscilloscope. In this way a very quick triggering is obtained because the signal way by-passes several circuits in the delay counter circuit. In this way it is possible to see the phenomena, on which triggering occured, in real time on the oscilloscope.

3.2.3. Micro processor system

The micro-processor system controls the entire timing and communication in the logic analyzer circuit.

The blockdiagram of the microprocessor system is given below:

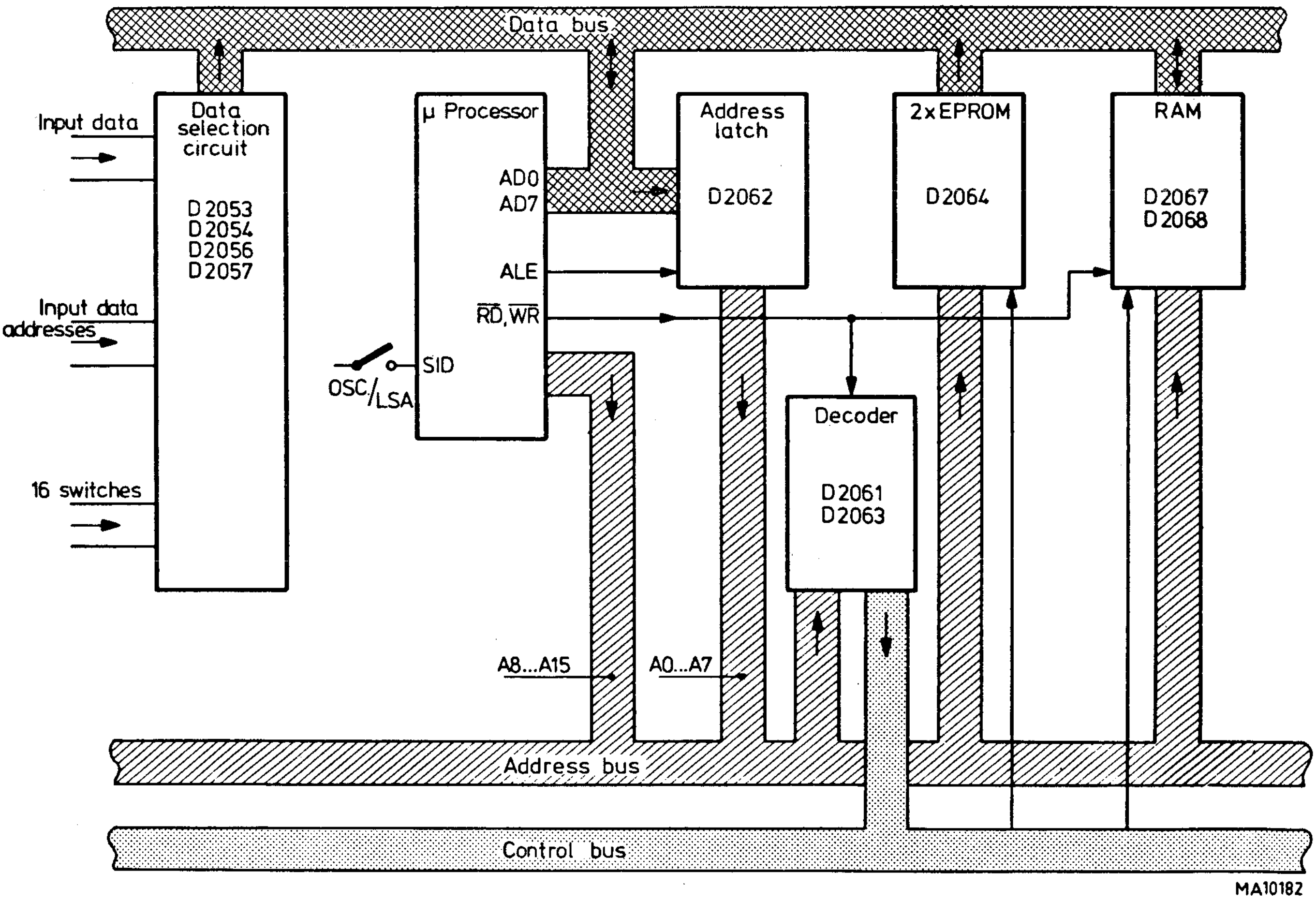

Data bus
Input data
Data selection circuit
D2053
D2054
D2056
D2057
Input data addresses
16 switches
µ Processor
AD0
AD7
ALE
$\overline{RD}$,$\overline{WR}$
SID
OSC/LSA
Address latch
D2062
2xEPROM
D2064
RAM
D2067
D2068
Decoder
D2061
D2063
A8...A15
A0...A7
Address bus
Control bus
MA10182

Fig. 3.2. Micro-processor system

3.2.3.1. µProcessor D2059

The µProcessor 8085 type controls the action in the LSA with the aid of the control signals, data bus and address bus.
The µProcessor has a 6 MHz crystal input to provide an internal clock signal. It is able to accept data, to interprete it and to decide, it is able to make arithmatical and logical operations on the data which is input.
After processing data will be output.

3.2.3.2. Address latch D2062

The µProcessor has a multiplexed Address-Data bus.
To separate the addresses from the data the AD0-AD7 signals are latched by the signal ALE from µProcessor.
The latch is a 74LS273 D type latch.
The address bus selects the location (in memory or a particular peripheral device) on which the data is read or written by µProcessor.

3.2.3.3. PROM D2064A & D2064B

The PROM circuit consists of two 2716 EPROM's (2Kx8 each).
They are pre-programmed and countain the software programmes on which the microprocessor D2059 operates.

3.2.3.4. RAM D2067 & D2068

The RAM circuit consists of two 256x4 static RAM's (Am9111) in parallel to form one 256x8 memory.
In this memory the μProcessor can store temporarily data for later processing. The RAM circuit is controlled by the control signals $\overline{\text{READ}}$, $\overline{\text{WRITE}}$ and $\overline{\text{RAM}}$.
This circuit serves also as reference memory for data which has to be compared in the COMPARE mode.

3.2.3.5. Decoder circuit D2061 & D2063

The decoder circuit consists of 2x74LS138 (1 to 8) decoders (each selectable) which decode the output address lines A11, A12 and A13 of the μProcessor and convert them to control signals.
When the μProcessor wants to read data from or to write data into a particular memory location or a particular peripheral device, the μProcessor generates an address and puts it on the address bus. The addresses A12-A12-A13 are sent to both the decoders D2061 and D2063. If for instance we want to read from PROM 2 (i.e. D2064B) the following addresses are outputed:
Address A15 is made "0" to achieve enabling of decoder D2061.
The address lines A13-A12-A11 are made 0 0 1 to choose output 1 of decoder S2061, which is the enable or read signal of PROM 2.
At the time this read signal is low (i.e. PROM 2 signal) PROM 2 will be activated. With the address lines A0 to A10 a memory location in the activated PROM is selected.
The address line A14 is not used in the system. The in the decoder circuit generated control signals and their specific addresses are given in the following table (i.e. Fig. 3.3.).

	ADDRESS BUS																	CONTR. BUS		NOTES
NAME OF SIGNAL	HEX	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00	$\overline{\text{WR}}$	$\overline{\text{RD}}$	X = DON'T CARE
$\overline{\text{PROM-1}}$	0000 07FF	0	–	0	0	0	X	X	X	X	X	X	X	X	X	X	X	1	0	– = NOT CONNECTED
$\overline{\text{PROM-2}}$	0800 0FFF	0	–	0	0	1	X	X	X	X	X	X	X	X	X	X	X	1	0	L/S = LEAST SIGNIFICANT
$\overline{\text{RAM}}$	1000 10FF	0	–	0	1	0	–	–	–	X	X	X	X	X	X	X	X	0/1	1/0	M/S = MOST SIGNIFICANT
$\overline{\text{CLDIM}}$	1800	0	–	0	1	1	–	–	–	–	–	–	–	–	–	–	–	0	1	
$\overline{\text{STRDI}}$	2000	0	–	1	0	0	–	–	–	–	–	–	–	–	–	–	–	0	1	
$\overline{\text{LATCH}}$	8000	1	–	0	0	0	–	–	–	–	–	–	–	–	–	–	–	0	1	
L/S $\overline{\text{RDIM}}$	8980	1	–	0	0	1	–	0	1	1	0	X	X	X	X	X	X	1	0	READ only D2018 L/S
M/S $\overline{\text{RDIM}}$	8A80	1	–	0	0	1	–	1	0	1	0	X	X	X	X	X	X	1	0	READ only D2019 M/S
L/S $\overline{\text{TRIGW}}$	9100	1	–	0	1	0	–	0	1	X	X	X	X	X	X	X	X	0	1	WRITE only 2009
M/S $\overline{\text{TRIGW}}$	9200	1	–	0	1	0	–	1	0	X	X	X	X	X	X	X	X	0	1	WRITE only 2011
+ M/S L/S $\overline{\text{DELAY}}$	9900	1	–	0	1	1	–	0	1	–	–	–	–	–	–	–	–	0	1	LOAD M/S BYTE
L/S $\overline{\text{DELAY}}$	9A00	1	–	0	1	1	–	1	0	–	–	–	–	–	–	–	–	0	1	LOAD L/S BYTE
MATRIX-0	A000	1	–	1	0	0	–	–	–	0	0	–	–	–	–	–	–	1	0	READ MUX. SWITCH
MATRIX-1	A040	1	–	1	0	0	–	–	–	1	0	–	–	–	–	–	–	1	0	READ MUX. SWITCH
L/S $\overline{\text{RDIM}}$=MTRX-2	8980	1	–	0	0	1	–	0	1	1	0	X	X	X	X	X	X	1	0	READ MUX. D2018 L/S
M/S $\overline{\text{RDIM}}$=MTRX-2	8A80	1	–	0	0	1	–	1	0	1	0	X	X	X	X	X	X	1	0	READ MUX. D2019 M/S
MATRIX-3	A0C0	1	–	1	0	0	–	–	–	1	1	–	–	–	–	–	–	1	0	READ MUX. DIM. ADR.
ASCII	A800	1	–	1	0	1	–	–	–	–	–	–	–	–	–	–	–	0	1	WRITE CHARACTER
Y-STDAC	B100	1	–	1	1	0	–	0	1	–	–	–	–	–	–	–	–	0	1	WRITE DAC-Y
Z-STDAC	B200	1	–	1	1	0	–	1	0	–	–	–	–	–	–	–	–	0	1	WRITE DAC-Z
X-STDAC	B300	1	–	1	1	0	–	1	1	–	–	–	–	–	–	–	–	0	1	WRITE DAC-X

MA10163

Fig. 3.3. Table of generated control signals

Remarks on table:

General : A11-A12-A13 and A15 are decoded to generate control and chip select signals.
A0...A10 are used to address a particular memory location.
A8 and A9 are also used for selecting the least- or the most significant byte of a data word (in case of 2 byte data transfer).
A6 and A7 are also used as selecting signals to control the output of the multiplexer circuit (D2053...D2057).

$\overline{\text{PROM 1}}$: Prom 1 is selected at address 0000H because of the programcounter of the µProcessor starts at this address after a reset. So it is obvious that this address must contain an upcode.

$\overline{\text{PROM 2}}$: A0-A10 are used to select the addresses in Prom 1.
When there is an overflow (at address 07FFH) the program counter continues at 0800H.
In this address the Address line A11 gets a high level. If we select Prom 2 with this address the memory map of PROM 1 and PROM 2 are sucessively.

$\overline{\text{RDIM}}$: L/S RDIM addresses from 8980H to 89BFH (i.e. 64 locations).
M/S RDIM addresses from 8A80H to 8ABFH (i.e. 64 locations).
Due to the program one of these addresses are stored in a register pair H and L in the µProcessor. If for instance 84H is stored in register H and 80H is stored in register L we can read data from the M/S Data Input Memory by an instruction "MOV A, M". In this way the contents of the memory location, addressed by register pair H.L. is loaded in register A of the µProcessor.
If we want to read from the L/S part of the Data Input Memory, it is possible to decrement the register H by the instruction "DRC H". The contents of reg H, which was 8AH, is decremented by one, resulting in 89H. This means that Address Line A9 is changed from the "high" into a "low" state. After this instruction a next "MOV A, M" reads automatically from the L/S part of the Data Input Memory.

$\overline{\text{MATRIX}}$ N : With this (address) signal, the Data Selection Multiplexers (D2053-D2054-D2056-D2057) are selected. With the addresses A6 and A7 we can select one of the four 8 bit inputs of the multiplexer.

	A7	A6	
$\overline{\text{Matrix 0}}$ =	0	0	= Read position front panel switches
$\overline{\text{Matrix 1}}$ =	0	1	= Read position front panel switches
$\overline{\text{Matrix 2}}$ =	1	0	= $\overline{\text{RDIM}}$
$\overline{\text{Matrix 3}}$ =	1	1	= Read DIM addresses

$\overline{\text{DELAY}}$: If we want to load the M/S part of the delay counter, the signal M/S $\overline{\text{DELAY}}$ (= 9900H) is generated.
With this signal the L/S part is also loaded but this part is reloaded with the right value with the signal L/S $\overline{\text{DELAY}}$ (= 9A00H). Because of the fact that the P.C. counter in the 8085 µProcessor counts up, it is obvious that the M/S part must always be loaded before the L/S part.

$\overline{\text{STDAC}}$: $\overline{\text{Z-STDAC}}$: $\overline{\text{STDAC}}$ signal together with Address line A8 is low. It is meant to start the 47 counter and load the ASC11 latch.
: $\overline{\text{Y-STDAC}}$: Is meant to store the vertical position of a character.
: X-STDAC : Is meant to store the horizontal position of a character on line. This signal is also activated at the time a $\overline{\text{Y-STDAC}}$ is generated. After a vertical position storage the horizontal position has to be reloaded with the proper value (similar to the DELAY signal).

3.2.3.6. Data Selection Multiplexer's D2053, D2054, D2056 & D2057

All information that the µProcessor must have from outside the microprocessor system is accepted via 4x 74LS253 multiplexers.
Each 74LS253 multiplexer consists of two 4-line to 1-line selectors (thus in total, eight 4-line to 1-line selectors).
The databus has only 8-bits (i.e. one byte) and because the "information" from outside the µProcessor is exceeding 8-bits, the data has to be multiplexed.
This occurs under control of the gated control signals $\overline{\text{MATRIX}}$ & $\overline{\text{RDIM}}$.
From which of the four input lines (of each selector) the "Information" is put through is determined by the addreeses A6 and A7 on the multiplexer.

Incoming data is:

Captured data from the Data Input Memory	8 bits
Addresses of the captured data (coming from addresscounter)	6 bits
Start/Stop signal $\overline{\text{(WRAM)}}$	1 bit
Action signal (i.e. gated signals of the switches: Down/Up, Right/Left, 1, X and 0)	1 bit
Position signal of 16 front panel switches	16 bits

The position of the LSA/OSC switch enters the μProcessor system via the 'SID input on D2059. There was no input left at the multiplexer for this signal. SID input is read by μProcessor with a RIM instruction.

3.2.4. Character generation

The block diagram of this circuit is given below:

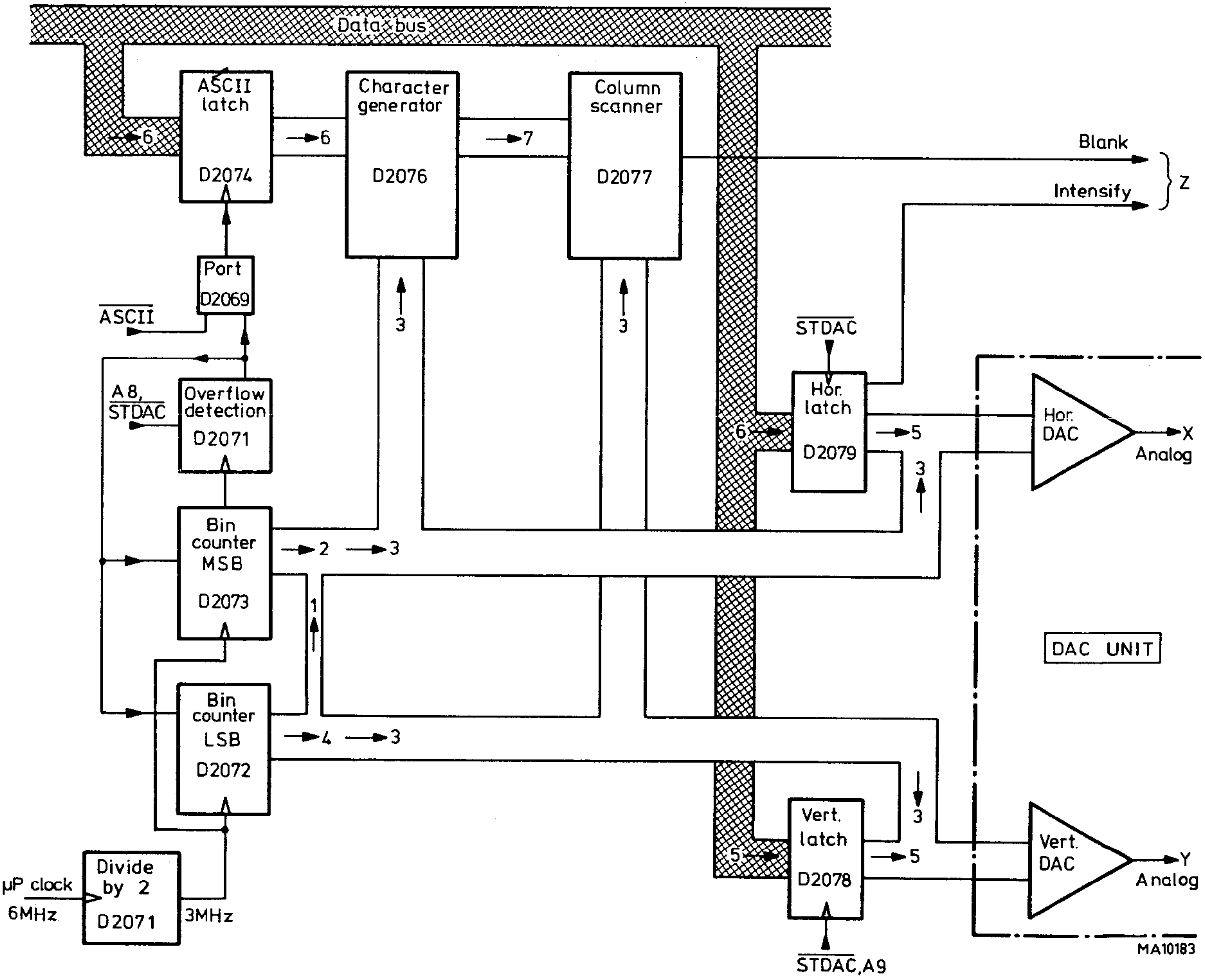

Data bus
ASCII latch
D2074
6
Character generator
D2076
6
Column scanner
D2077
7
Blank
Intensify
Z
Port
D2069
ASCII
3
3
STDAC
A8, STDAC
Overflow detection
D2071
Hor. latch
D2079
6
5
3
Hor. DAC
X
Analog
Bin counter MSB
D2073
2
3
1
DAC UNIT
Bin counter LSB
D2072
4
3
3
Vert. latch
D2078
5
5
Vert. DAC
Y
Analog
μP clock 6MHz
Divide by 2
D2071
3MHz
STDAC,A9
MA10183

Fig. 3.4. Display circuit

The character generation circuit processes the output from microprocessor system to produce a visual display on the CRT of the data captured from the system under test.

3.2.4.1. Character Generator D2076

This is a ROM Containing the alpha-numeric characters as used in the PM 3540. Each character is stored in a memory field of 6x8 bits.

This means that for every character 6 memory locations are used. A character is composed of 6 columns vertically (i.e. each memory location) and 8 bits horizontally).

See Fig. 3.5. for the memory cap of this ROM.

ASCII code	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	G0	G1	G2	G3	G4	G5	G6	G7	
																			not used
40H	1	0	0	0	0	0	0												
41H	1	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	character A
								0	0	1	1	1	1	1	1	0	0	0	
								0	1	0	0	0	0	1	0	1	0	0	
								0	1	1	0	0	0	1	0	0	1	0	
								1	0	0	0	0	0	1	0	1	0	0	
								1	0	1	1	1	1	1	1	0	0	0	
								1	1	0	0	0	0	0	0	0	0	0	not used
								1	1	1	0	0	0	0	0	0	0	0	
42H	1	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	character B
								0	0	1	1	0	0	0	0	0	1	0	
								0	1	0	1	1	1	1	1	1	1	0	
								0	1	1	1	0	0	1	0	0	1	0	
								1	0	0	1	0	0	1	0	0	1	0	
								1	0	1	0	1	1	0	1	1	0	0	
								1	1	0	0	0	0	0	0	0	0	0	not used
								1	1	1	0	0	0	0	0	0	0	0	
	not present							0	0	0	0	0	0	0	0	0	0	0	next character

MA10162

Fig. 3.5. Character presentation

With the highest 6 address lines we choose the memory field in which a certain character is stored. This address is coded in the ASCII code, i.e. with A8, A7, A6, A5, A4, A3 = 01H, for the letter "A". The "one's" represent the character(s) in the display.

The real ASCII code for "A" is 41H but the most significant bit (A9) of the address is left out (see Fig. 3.5).

With the 3 least significant address lines we choose a column of a character.

In the ROM the character field (A3 to A8) is chosen by the μProcessor (via ASCII latch D2074) and the columns are scanned by the 3 most significant bytes of the 47 (57 oct) counter.

A character is generated as follows:

The μProcessor stores a ASCII code in D2074 (HEF 40174 D type latch).

The latch in turn chooses the character field in the character generator ROM.

The 47 counter is starting at its maximum count and counts down, which means that we start at A2.A1.A0 = 101 (47 Dec = 57 oct = 101 111 bin) and are the lower address bits of the character generator (see Fig. 3.5.).

These address bits are used to address the different columns of a character.

Each column of a character is outputted to the multiplexer D2077. While the 47 counter is running, this column is scanned by D2077 until the most significant 3 bytes fo the 47 counter changes its state. At that time the next column is outputted to D2077 and is again scanned by the 47 counter etc. etc.

3.2.4.2. *Column scanner D2077*

Which is a 74LS151 multiplexer. The input is an 8 bit word (column) from character generator. By means of 3 address inputs each bit can be outputted to pin 5 (Data selector principle). In this way the 8-bits of a character column are outputted one by one to the blanking input of the CRT. A high level (logical "1") at D2077's output means an illuminated spot on the screen. A zero means a dark spot. In this way the binary form of a character can be made visible. There is also port D2008 (which output signal is applied, via X23, to the Z-Modulation input D1203 in the horizontal ampl.) to make sure that the Z-Modulation is on in oscilloscope mode.

3.2.4.3. *The 47dec Counter D2072 and D2073*

The counter is composed of two HEF 4029 binary counters.

They are intended to scan the column's of a character (3 M/S bits) and the bits of a column in a character (3 L/S bits). In the meantime these 6 outputs are also used to deflect the electronbeam of the CRT to bring the illuminated and blanked spots on the right place on the screen. For this reason the 3 M/S bits are fed to the horizontal DAC and the 3 L/S bits to the vertical DAC.

3.2.4.4. Divide by TWO and OVERFLOW detection (D2071) and PORT (D2069)

The counting is controlled as follows:
The counter is started by control signal $\overline{\text{STDAC}}$ (together with A8 = 0) at reset input (pin 1) of D2071 (74LS74 D-flip-flop). At this time the load signal for the 47 counter, which has loaded the counter with 47D is omitted. Now the counter can count on clock pulses from the D2071 output (pin 9), which devides the µProcessor clock UPCLK (which is 3 MHz) by two. Now the counter is running from 47D to 0 (representing the 48 bits of one character).
When the counter passes the zero state the overflow detection (D2071 pins 1...6, which is ½ 74LS74 D-type flip-flop) is clocked and generates a load signal for the counter to load with 47.
This load signal remains until the µProcessor releases it by the signals $\overline{\text{STDAC}}$ and A8, as described at the beginning of this paragraph.
As the counter is free running it has to be synchronized with the µProcessor output to the character generator. For instance when the µProcessor has processed a new character and wants to output it to the ASCII latch (D2074) it is possible that the preceeding character is not yet completely executed.
When the µProcessor wants to load the ASCII latch (D2074) by control signal ASCII at the time the counter is still running, the µProcessor is forced to the not ready or wait state by a low signal at port D2069 pin 11, which is connected with the READY input of the µProcessor (D2059). When the counter is ready (noticed by the overflow of the detection circuit) the output of port D2069 pin 11 will be high and enables the ASCII latch. The READY input of the µProcessor is high again, which means that the µProcessor proceeds to execute the preset instruction.

3.2.4.5. Horizontal latch D2079 and horizontal DAC

As it is possible to select (i.e. positioning) the columns of a character with the 3 M/S bits of the 47 counter it is also possible to deflect the electron beam of the CRT with these same signals.
But for this the digital "information" has to be converted to an analogue signal. This is done by using a ladder network of resistors, weighted in a binary fashion. This means that the resistors are chosen at that value that the least significant bit causes a current half of that from the next bit which is in its turn producing a current half of that of the significant bit of the three. The simplified circuit is shown in Fig. 3.6. below:

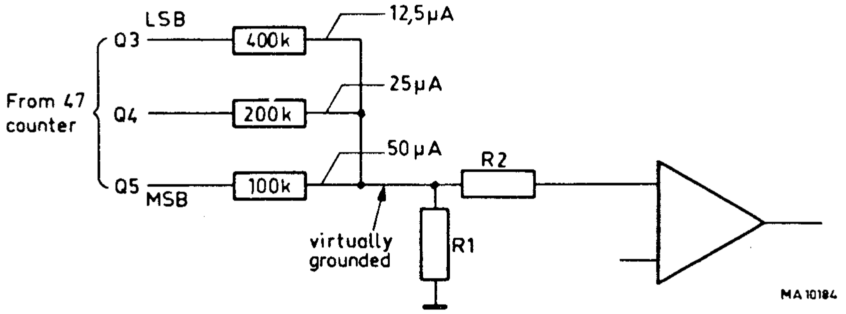


Fig. 3.6. Binary weighted resistor "ladder" DAC

Q3 causes a current of $\frac{5\ V}{400\ K\Omega}$ in which 5 V is the output voltage of the 47Dec counter.
The resistors R1 and R2 are necessary to adjust the total current contribution of the 3 M/S bits of the 47Dec counter to the rest of the horizontal DAC circuitry.
The reason for this is that the resistors could not be made greater due to the capacitive load of the counter. These resistors only produce the horizontal deflection within the character.

The position of a character on a horizontal line on the screen is determined by the X-latch D2079 and its digital to analogue converter.
The horizontal latch is controlled by the µProcessor by means of the control signal $\overline{\text{STDAC}}$. With this signal the digital information for the horizontal position is stored in D2079, which is a HEF 40174,D type latch. The digital information is converted into an analogue signal form (i.e. current) and added to the horizontal signal coming from the 47Dec counter.
The digital to analogue convertor used for this is a R-2R resistor (latter) network.

The simplified circuit is shown in Fig. 3.7. below:

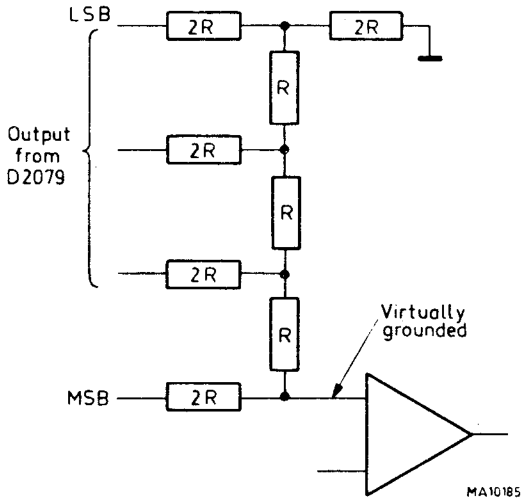


Fig. 3.7. Binary R-2R "ladder" DAC

From the calculated contribution of each output it can be seen that each output contributes half the current of its next more significant bit, thus equivalent to its bit weight (e.g. 2^3, 2^2, 2^1, 2^0 etc.).
It is obvious therefore, that the circuitry, as used in fig. 3.6. cannot be used because the most significant output would then have a resistor which is too small in proportion to the internal resistor of the horizontal latch. (which is between 250 Ω and 1000 Ω).

The horizontal latch D2079 has also another function. One bit (pin 11) is preserved to latch the intensity information.
Each time a character is positioned by μProcessor it also stores the information whether the character has to be displayed or not (i.e. in case of a cursor or an in equality in the COMPARE mode). If an "1" is stored in the latch an extra current is pushed into the Z amplifier of the CRT control.
In case of a "0" is stored a current is taken fromthe Z amplifier, during this time the particular screen position is blank.

3.2.4.6. *Vertical latch D2078 and Vertical DAC*

Description of the vertical latch and digital to analogue converter are similar to the horizontal latch and DAC. The vertical latch is positioning the electron beam on a vertical line on the screen and is controlled with the gated $\overline{\text{STDAC}}$ and A9 signal.
Gating takes place in the OR gate D2069 pins 4, 5, 6.

3.2.5. Software Overview

The full software listing for the PM 3540 is complex and beyond the scope of this manual, for this reason flow diagrams, Fig. 3.8. and Fig. 3.9. are provided to give a software overview of the data capture and display actions which directly affect the related hardware within the PM 3540.

Fig. 3.8. A state by stage flow diagram of data capture, comparison, calculations of display and delay routines.

Fig. 3.9. An expansion of the display routine stage (shown in fig. 3.8.) giving details of the display mode, character generating, D.A.C.'s and blanking routines.

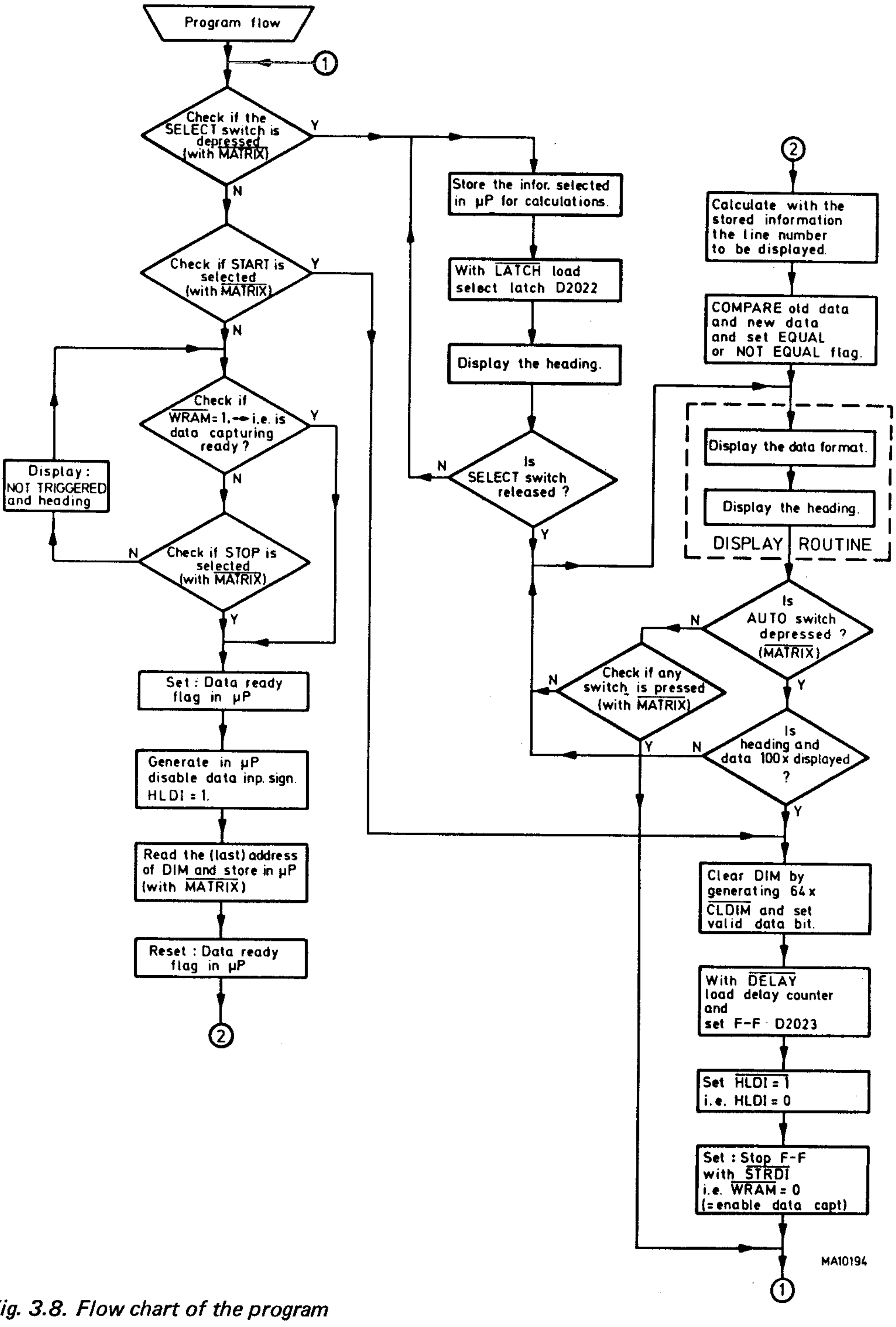

Program flow
①
Check if the SELECT switch is depressed (with MATRIX)
Y
N
Check if START is selected (with MATRIX)
Y
N
Check if WRAM = 1.→ i.e. is data capturing ready ?
Y
N
Display : NOT TRIGGERED and heading
Check if STOP is selected (with MATRIX)
N
Y
Set : Data ready flag in µP
Generate in µP disable data inp. sign. HLDI = 1.
Read the (last) address of DIM and store in µP (with MATRIX)
Reset : Data ready flag in µP
②
Store the infor. selected in µP for calculations.
With LATCH load select latch D2022
Display the heading.
Is SELECT switch released ?
N
Y
②
Calculate with the stored information the line number to be displayed.
COMPARE old data and new data and set EQUAL or NOT EQUAL flag.
Display the data format.
Display the heading.
DISPLAY ROUTINE
Is AUTO switch depressed ? (MATRIX)
N
Y
Check if any switch is pressed (with MATRIX)
N
Y
Is heading and data 100x displayed ?
N
Y
Clear DIM by generating 64x CLDIM and set valid data bit.
With DELAY load delay counter and set F-F D2023
Set HLDI = 1 i.e. HLDI = 0
Set : Stop F-F with STRDI i.e. WRAM = 0 (=enable data capt)
MA10194
①

Fig. 3.8. Flow chart of the program

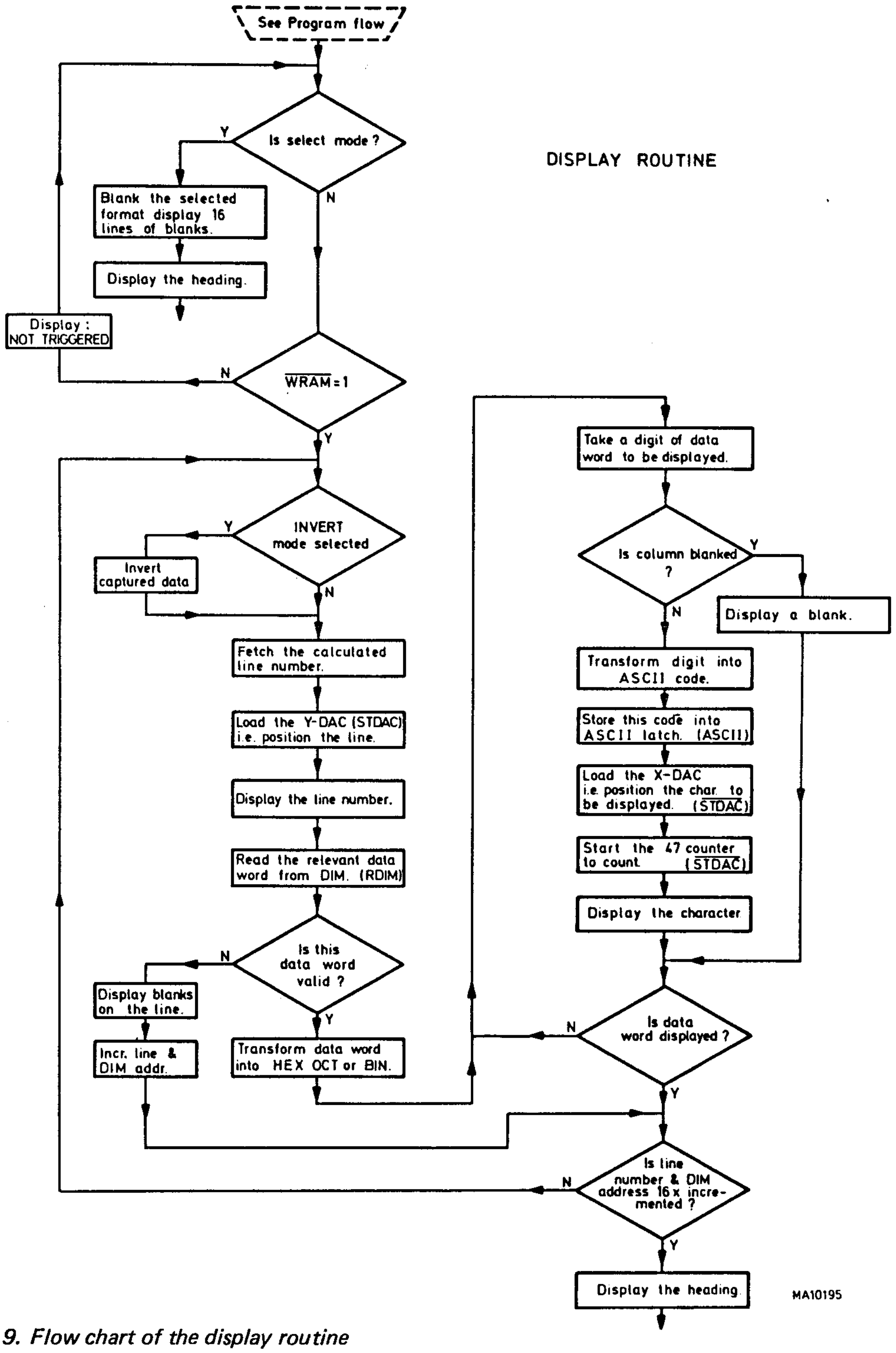

See Program flow
DISPLAY ROUTINE
Is select mode ?
Y
N
Blank the selected format display 16 lines of blanks.
Display the heading.
Display : NOT TRIGGERED
$\overline{\text{WRAM}}=1$
N
Y
INVERT mode selected
Y
N
Invert captured data
Fetch the calculated line number.
Load the Y-DAC (STDAC) i.e. position the line.
Display the line number.
Read the relevant data word from DIM. (RDIM)
Is this data word valid ?
N
Y
Display blanks on the line.
Incr. line & DIM addr.
Transform data word into HEX OCT or BIN.
Take a digit of data word to be displayed.
Is column blanked ?
Y
N
Display a blank.
Transform digit into ASCII code.
Store this code into ASCII latch. (ASCII)
Load the X-DAC i.e. position the char. to be displayed. ($\overline{\text{STDAC}}$)
Start the 47 counter to count. ($\overline{\text{STDAC}}$)
Display the character
Is data word displayed ?
N
Y
Is line number & DIM address 16 x incremented ?
N
Y
Display the heading
MA10195

Fig. 3.9. Flow chart of the display routine

3.2.6. Circuit description of the oscilloscope part

3.2.7. Vertical deflection system

The vertical channels A and B are identical, each comprising an input coupling switch, an input step attenuator, an impedance converter and a preamplifier with trigger pick-off.
A channel multivibrator, controlled by the display mode pushbuttons, switches either channel A or channel B to the final Y amplifier via the delay line driver and the delay line. The final Y amplifier feeds the Y deflection plates of the cathode-ray tube.
The individual stages of the vertical deflection system are now described in detail.
As the signal paths for channel A and channel B are basically identical, only the channel B signal path is described.

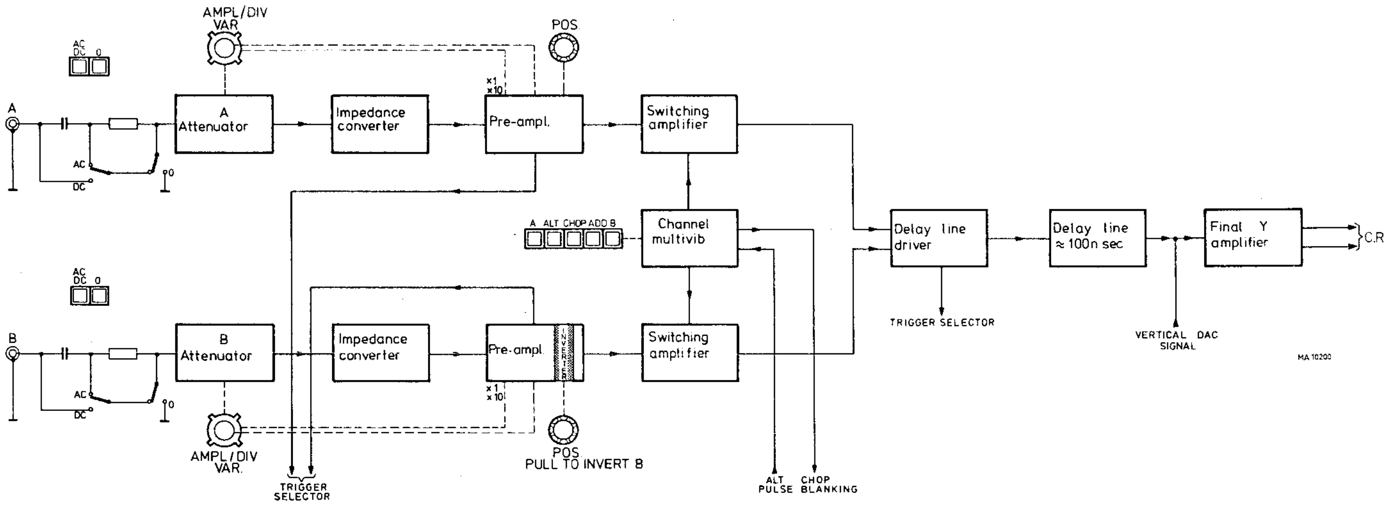

AMPL/DIV VAR
POS.
AC DC 0
A
AC
DC
0
A Attenuator
Impedance converter
x1 x10
Pre-ampl.
Switching amplifier
A ALT CHOP ADD B
Channel multivib
Delay line driver
Delay line ≈ 100n sec
Final Y amplifier
C.R.
TRIGGER SELECTOR
VERTICAL DAC SIGNAL
MA 10200
AC DC 0
B
AC
DC
0
B Attenuator
Impedance converter
Pre-ampl.
INVERTER
x1 x10
Switching amplifier
AMPL/DIV VAR.
POS. PULL TO INVERT B
TRIGGER SELECTOR
ALT PULSE
CHOP BLANKING

Fig. 3.10. Vertical deflection system

3.2.7.1. Input coupling

Input signals connected to the B input socket X3 can be a.c. coupled, d.c. coupled or internally disconnected.
In the AC position of S14, there is a capacitor (C401) in the signal path. This capacitor prevents the DC component of the input signal from being applied to the amplifier.
In position DC of switch S14, the input signal is coupled directly to the step attenuator.
At the same time, blocking capacitor C401 is discharged via R402, to prevent damage of the circuit under test by a possible high charge.
S15 (0) isolates the B input signal and earths the channel input for reference purposes; e.g. for calibration or centering the trace.

3.2.7.2. Input attenuator

The input attenuator is a frequency-compensated, high-impedance voltage divider with twelve positions. The overall attenuation of the stage is determined by the combination of the selected sections of two voltage dividers. The various combinations are selected by the twelve positions of the frontpanel AMPL/DIV attenuator switch S8.
The first divider sections attenuate by factor of 1.25, 3.125 and 6.25 and the second divider sections attenuate by a factor of 1x, 10x and 100x.
With the overall combinations of attenuation, nine Y deflection coefficients are realised from 20 mV/div to 10 V/div in a 1-2-5-sequence. Only for the most sensitive positions 2 mV/div, 5 mV/div and 10 mV/div of AMPL/DIV attenuator switch S8, the gain of the Y amplifier is increased by a factor of 10.
The input capacitance of the attenuator cannot be adjusted in the individual positions. Small differences of approx. 1 pF are allowed.
The voltage divider sections are made independent of the input frequency over the frequency range of the oscilloscope (i.e. 35 MHz) by means of the trimmers C407, C413, C416, C417, C418 and C419.

3.2.7.3. *Impedance converter*

The impedance converter is formed by V604 (two matched field-effect transistors). The two FET transistors are used in source follower configuration.
The signal level on the gate (and on the source) of the upper FET amounts to 1.6 mV/div or 16 mV/div.
Diode V601 together with the output impedance of the attenuator and also the attenuator action protects the input source follower, against excessive negative input signals. The d.c. balance of the circuit can be adjusted with R604, providing attenuator balance for the 10 mV/div and 20 mV/div positions.

3.2.7.4. *Preamplifier*

The input stage formed by D601 (5 transistors) is switched ina Cherry-Hooper configuration and direct coupling is employed throughout.
In the positions 20 mV/div — 10 V/div of the AMPL/DIV switch S8, contact K601 is open and the gain is determined by

$$\frac{R628 + R632}{R611 + R612} = \text{approx. } 1{,}8\text{x}$$

If K601 is closed (in positions 2 mV/div, 5 mV/div and 10 mV/div) the gain of this stage is increased by a factor of 10. This is accurately adjusted with R621.
To prevent jumping of the trace when K601 is switched with the input short circuited, no voltage must be present across these contacts. R604 (attenuator balance) serves this purpose.
R8 in conjunction with R622, R623, R624 and R626 forms the vernier control. In the calibrated position (R8 is 1 kohm) the transfer of this network is 0,85x. Wirh R8 to its minimum position (0 ohm) the transfer is 0,3x. Thus we have a control range of 3x.
V608, V609, V613, V614, V616 and V617 form a symmetrical cascode circuit supplying an output CURRENT to the channel switch.
The transfer conductance of this stage is:

$$\frac{I_{out}}{U_{in}} = \frac{1}{R641 \,//\, (R637 + R638) \,//\, (R646 + R647 + R648)} = 7 \text{ mA/V}$$

The signal level at the input of this stage is approx. 24 mV/div equivalent to approx. 170 µA/div at the output.

Note: The channel A gain can be equalised to the channel B gain with the aid of R543 (gain x1 in channel A amplifier).

3.2.7.5. *Trigger pick-off*

The trigger signal is picked-off at the emitters of V608 and V609, a signal source with a low internal resistance, by the series feed-back stage V611 and V612.
From this stage the trigger signal current is fed asymmetrically to the trigger selector via a 50 Ω cable.

3.2.7.6. *Normal invert switch*

The B channel has a provision for inverting the polarity of the Y signal. Push-pull switch S4, PULL TO INVERT B, is mounted on the shaft of front-panel control B POSITION. In the invert position of the switch the normal signal paths are blocked because V613 and V614 are switched off.
Inversion is achieved by V616 and V617 providing alternative paths for the signal when their bases are switched less positive by S4. Possible unbalance between the two positions of the switch can be compensated by preset potentiometer R647 (Norm invert balance).

3.2.7.7. *Position control*

Potentiometer R3 is the vertical POSITION control. Its balance is adjustable by means of R674 (shift balance).

3.2.7.8. *Channel multivibrator*

The channel multivibrator consists of two circuits which are inserted in the A and B channel signal paths.
The A channel circuit consists of the transistors V524, V526 and the diodes V521, V522 and V523. The B channel circuit consists of the transistors V624 and V626 and the diodes V621, V622 and V623.
When the junction of the three diodes is positive in relation to mass, the diodes are non-conductive. The transistors, and thus, the signal path are conductive.
If the current drained from the junction exceeds 6 mA, the diodes are conductive and the transistors are turned off.
The circuits are driven from the flip-flop formed by the transistors V703 and V704.

With A (S1) depressed: only channel A is displayed.
The base of V703 is connected to the −12 V supply voltage. V703 is turned-off then, its collector voltage is high and channel A is switched on. At the same moment channel B is switched off.

With ALT (S1) depressed: channels A and B are alternately displayed.
This push-button is a dummy and has no contacts, but it releases all the other push-buttons of the display-mode controls. In this mode there is a DC path via R704 between the two emitters, the circuit is bi-stable and one of the diodes is conductive.
V1201 is not conducting in ALT mode and negative going alternate pulses derived from the time-base generator are fed to the circuit. These pulses switch the circuit at the end of each sweep and the channels A and B are alternately displayed.

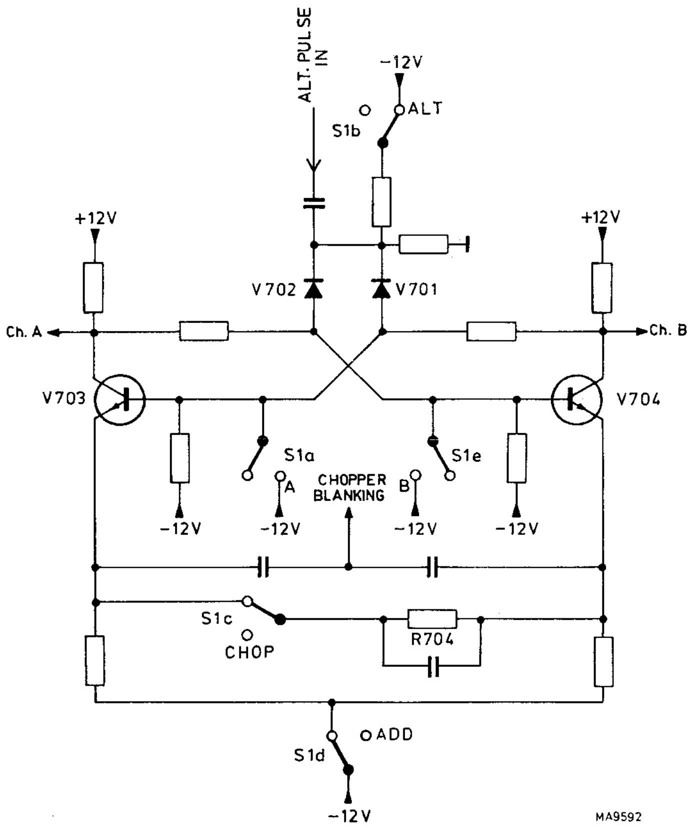


Fig. 3.11. Simplified diagram of the channel multivibrator

In the ALT mode −12 V is applied via S1 (A), S1 (CHOP), S1 (ADD) and S1 (B) and R710 to transistor V1506 in the beam blanking amplifier.
This transistor is then blocked and the only control signal for the beam unblanking amplifier is the normal unblanking pulse coming from the time-base circuit.

With CHOP (S1) depressed: channels A and B are chopped.
In this mode the circuit acts as a chopper generator. S1 is open then, the DC path between the emitters of V703 and V704 is interrupted and the circuit is a-stable. Both diodes V701 and V702 are then turned-off and the circuit starts oscillating, the oscillating frequency being approx. 500 kHz.
During the switching transients in the CHOP mode, the c.r.t. is blanked with the aid of differentiated chopper blanking pulses (at the junction of R703 and C702) which are fed to the Z-amplifier.

With ADD (S1) depressed: channel A and B are added.
Both transistors are turned-off, both collector voltages are high and both channels are switched on.

With B (S1) depressed: only channel B is dislayed.
The base of V704 is connected to the −12 V supply voltage. V704 is then turned-off, its collector voltage is high and channel B is switched on. At the same moment channel A is switched off.

3.2.7.9. *Delay line driver*

The symmetrical delay line is sandwiched between a series feed-back push-pull amplifier and a shunt feed-back push-pull amplifier, consisting of integrated circuit D801.
This amplifier combination is called "CHERRY-HOOPER" circuit.
The series feed-back stage receives a signal of approx. 30 mV/div which is obtained from a signal current of 0.17 mA/div from the channel switch, multiplied by the value of the load resistance R803 + R804 = 200 Ω.
The emitter impedance of the series feedback stage consists besides RE = R819 + R821 of the parallel circuit of a number of RC networks. As the delay line is a source of distortion for higher frequencies, these networks provide the necessary delay line compensation.
At the input side, delay line D802 terminates in R828 and R829 (totally 200 Ω).
The delay line itself is a symmetrically mounted spiralized cable with a characteristic impedance of 200 Ω and a delay of 110 nsec/m. At the output side, the cable terminates via R831 and R832 in the virtual earth points of the shunt feed-back stage. The input impedance on these virtual earth points is 14 Ω. This value in series with the 86.6 Ω of R831 and R832 forms the correct termination for the delay line. C814 and C816, used for HF correction, are also the points to which the output signals of the vertical D.A.C. are fed.

3.2.7.10. *Composite trigger pick-off*

The composite trigger signal is picked-off at the emitters of the series feed-back stage (D801), a amplifier with a low emitter resistance, due to the series-feedback by V802 and V803. From the collector of V803 the composite trigger signal current is fed to the trigger selection switch (S16) via a 50 Ω cable.

3.2.7.11. *Final Y amplifier*

The output signals of the shunt feed-back stage are applied to the final Y amplifier stage consisting of the transistors V804, V806, V807 and V808, which are configured as two series feed-back amplifiers in parallel fed by a constant current source.
The gain of the final amplifier can be set by means of potentiometer R848. The centre taps of the coils L801 and L802 are connected to the Y deflection plates of the c.r.t. The Y deflection plates form filters together with the coils L801 and L802. These filters terminate in resistors R859, R861, R862 and R863.

3.2.8. **Triggering**

The trigger source switches for triggering the time-base generator, can select any of the following input sources:
- an internal signal from the vertical A channel
- an internal signal from the vertical B channel
- an internal composite signal of channel A and channel B
- a signal derived from the analyzer circuit
- an external source
- an external source combined with a signal derived from the analyzer circuit.

All these sources can be used for both triggering and X deflection purposes. Source selection is done by means of a trigger selector switch S16 that feeds the trigger signals to the trigger circuitry.

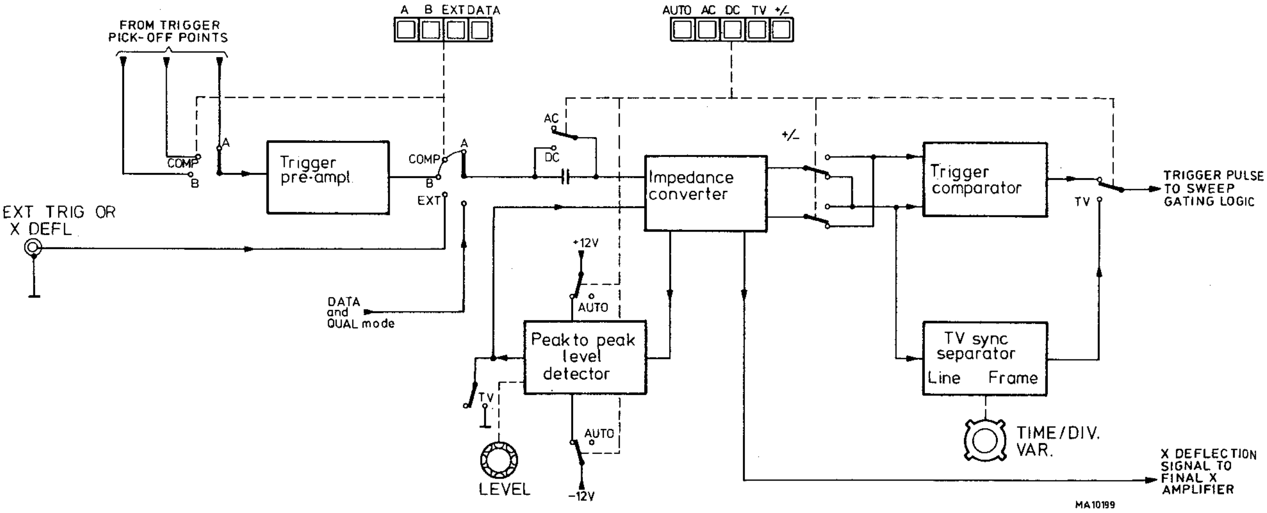

A
B
EXT
DATA
AUTO
AC
DC
TV
+/–
FROM TRIGGER PICK-OFF POINTS
COMP
A
B
Trigger pre-ampl
COMP
A
B
EXT
EXT TRIG OR X DEFL
DATA and DUAL mode
AC
DC
Impedance converter
+12V
AUTO
Peak to peak level detector
TV
LEVEL
AUTO
-12V
+/–
Trigger comparator
TV
TRIGGER PULSE TO SWEEP GATING LOGIC
TV sync separator
Line
Frame
TIME/DIV. VAR.
X DEFLECTION SIGNAL TO FINAL X AMPLIFIER
MA10199

Fig. 3.12. Trigger circuit

3.2.8.1. *Trigger source selection and preamplifier*

The signal currents (60 μA/div) of the three trigger pick-off stages (A, B and Comp) are, after selection by S16, amplified to a level of 100 mV/div by a shunt feed-back stage + emitter follower stage consisting of V351 and V352. After this stage there is a selection between its output signal, a signal on the external socket and a signal which is derived from the analyzer circuit. Signals that are not used are short-circuited to mass.

3.2.8.2. *Impedance converter*

The trigger signal of 100 mV/div is fed via the AC-DC coupling switch S2 to a FET (V1006) in source follower configuration.
From here the signal is applied via an emitter follower to the ± slope selection switch (part of S2). This selection switch enables triggering on either the positive-going or the negative going edge of the triggering signal.

3.2.8.3. *Trigger comparator*

From the ± slope selector switch the signal is fed via a common emitter amplifier D1001 (123/345) to the output shunt feed-back amplifier V1014 via the TV mode switch (S2). The voltage gain is high (28x) but its dynamic range is small (2.8 Vp-p at the output). This is because of the tail current of the symmetrical common emitter stage is 2 mA. The current sweep at the output of this stage is consequently 2 mA at max. which is transformed into a 2.8 V max. voltage sweep at the output of the shunt feed-back amplifier V1014. This means that the trigger amplifier is completely driven at a trace height of 1 div. Which division on the screen this is, depends on the position of the LEVEL control R5.
With AC (S2) or DC (S2) depressed, the range of the LEVEL control is fixed. The DC voltage at the wiper of LEVEL control R5, which is fed to the FET (V1006) can vary between +3.5 V and −3.5 V. Diodes V1001 and V1002 are then turned off, and the voltage on the gate of the FET is then adjustable between + 0.9 and −0.9 V. At a signal level on the gate of the other FET of 100 mV/div, there will be a control range of ± 9 div.

3.2.8.4. *Peak to peak level detector*

If the AUTO push-button (S2) is depressed, the supply voltages for the level control circuit are interrupted.
A trigger signal (300 mV/div) which is derived from the emitter follower stage and amplified by V1008, gives after peak to peak detection a DC voltage across the level control. This DC voltage is approx. proportional to the amplitude of the trigger signal. This is the auto trigger level control. The peak-to-peak level of the signal then determines the range of the level control.

3.2.8.5. *T. V. Synchronisation separator*

If the TV mode push-button (S2) is depressed, the LEVEL control is switched off. The wiper of R5 is then connected to mass. A synchronisation separator for the television signals is then inserted into the trigger signal path.

A composite video signal contains, besides the video information, also synchronisation pulses with line and frame frequency which can be distinguished by their pulse width.
The TV synchronisation separator circuit is able to:

1. separate the synchronisation pulses from the video information.
2. distinguish between frame synchronisation pulses and line synchronisation pulses.

The first requirement is met by V1013 acting as a DC restorer and limiter, the second requirement by the integrating network R1047, C1011 and C1012.
The TV signal is picked-off at the ± slope selector switch which in this case can be set for the right polarity of the TV signal. The TV trigger signal is then amplified by the series feed-back push-pull stage V1009, V1011 and applied to synchronisation separator V1013 via emitter follower V1012. The signal on the base of V1013 could be as follows:

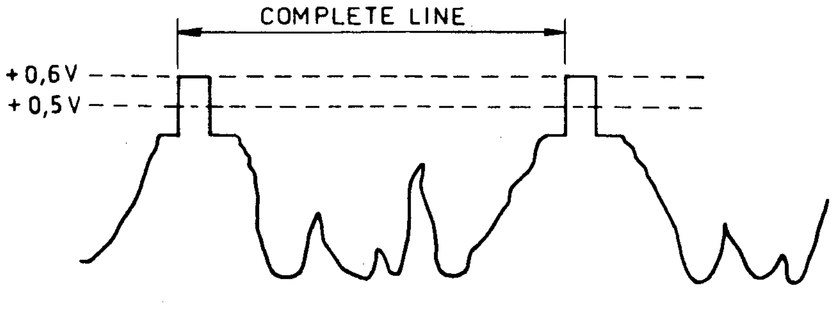


Fig. 3.13. Signal on the base of transistor V1013

The peaks of the synchronisation pulses are all held at one level by the DC restorer action of C1007, R1039 and the base emitter diode of V1013. The base voltage will never exceed +0.6 V by a large amount, but the complete waveform will appear at the base. The signal level is at this point approx. 280 mV per screen div. Change in signal of approx. 100 mV is sufficient to turn off V1013. V1013 looks only to the peaks of the synchronisation pulses.
The rest of the TV signal has no influence. On the collector of V1013 we find exclusively the synchronisation signal consisting of line synchronisation pulses and the wider frame synchronisation pulses.

In the time base positions 20 μsec/div and faster, this complete signal is transmitted to the time base generator and we have line triggering.
In the time base positions 50 μsec/div. and slower, C1011 and C1012 are connected to mass. The narrower line synchronisation pulses are then integrated out of the signal, but the wider frame synchronisation pulses remain, and frame triggering is obtained. A second threshold is built-up by V1016. V1017 reacts to the signal that still passes and consists of pure line or frame synchronisation pulses. After this the signal is fed to the time base generator via V1014.

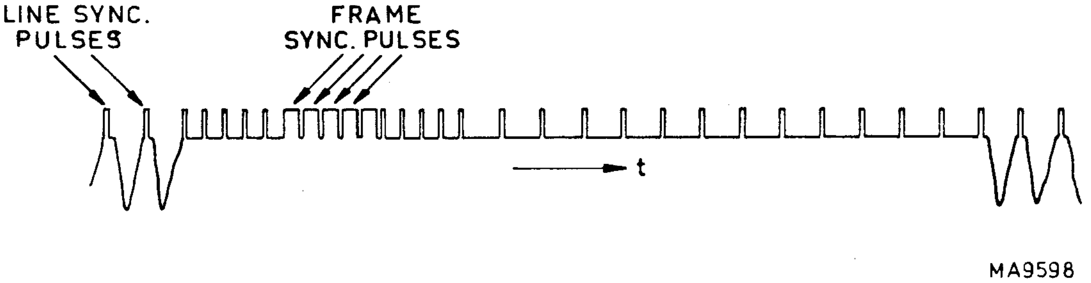

LINE SYNC. PULSES
FRAME SYNC. PULSES
t
MA9598

Fig. 3.14. A vertical interval with frame synchronisation pulse group

3.2.9. Time-base generator

The time-base generator comprises a sweep gating logic, a sweep generator, a hold-off circuit, an auto sweep circuit and X final amplifier.

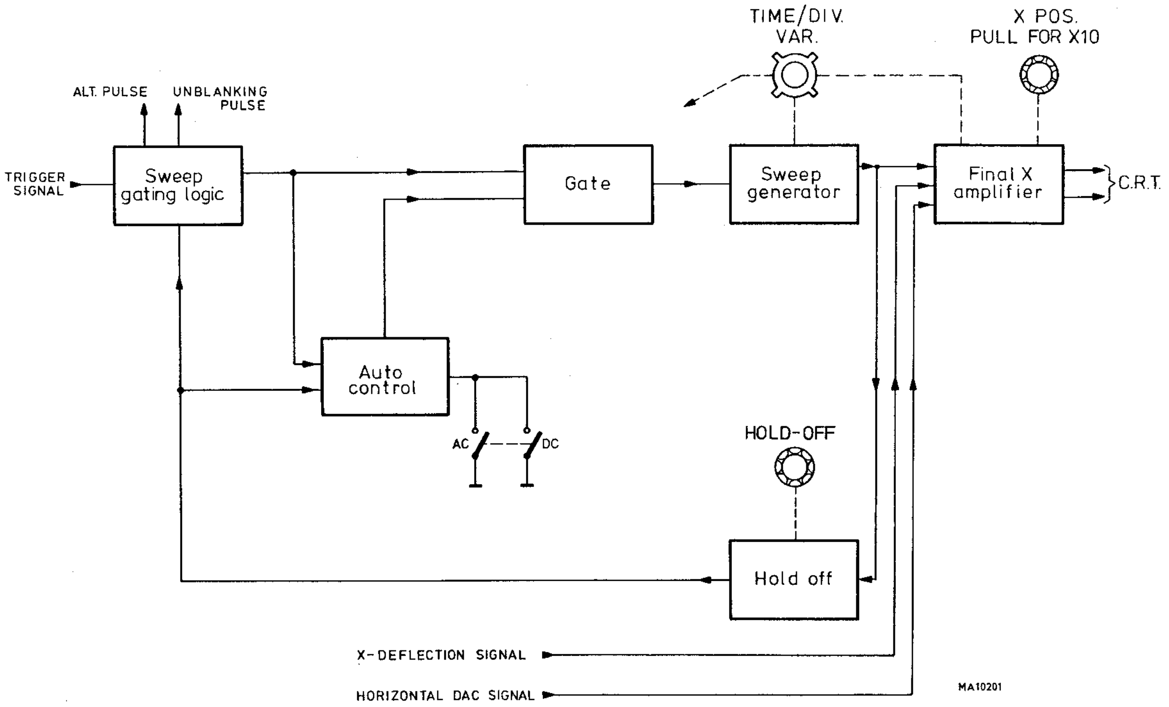

TIME/DIV.
VAR.
X POS.
PULL FOR X10
ALT. PULSE
UNBLANKING PULSE
TRIGGER SIGNAL
Sweep gating logic
Gate
Sweep generator
Final X amplifier
C.R.T.
Auto control
AC
DC
HOLD-OFF
Hold off
X-DEFLECTION SIGNAL
HORIZONTAL DAC SIGNAL
MA10201

Fig. 3.15. Time-base generator

Before considering these stages in detail, the general principle is briefly described. Basically, the sweep gating logic, under the control of trigger signals from the trigger comparator and feedback pulses from the hold-off circuit, supplies square-wave pulses to the switching transistor V1213 of the sawtooth generator.
The time-base capacitors (effectively in parallel with the switching transistor) are charged linearly through a constant-current source to provide the forward sweep then are discharged rapidly by the switching transistor to provide the flyback period. The resulting sawtooth is fed to the X-final amplifier.

3.2.9.1. Sweep generator

The sweep speed or time coefficient is determined by the value of the time-base capacitance in circuit and by the magnitude of the charging resistor selected.
The time-base capacitors are C1204 and C1207. Capacitor C1204 is always in circuit, C1207 is selected by the transistor V1216. This transistor operates as an electronic switch and is either fully cut-off or fully-conducting. It is switched on by the application of a positive voltage to its base from the TIME/DIV switch S10.
According to the position of S10, this transistor V1216 switches in the capacitor C1207 in parallel with C1204.
As mentioned, the sweep speed is also dependent upon the magnitude of the accurate constant-current supplied by transistor V1212. This current can be adjusted in steps by selecting the emitter resistance of V1212 by means of the TIME/DIV switch S10. Continuous control of the charging current can be effected by varying the base drive to V1212 with the continuous sweep control, TIME/DIV potentiometer R9. In the CAL position of this potentiometer, switch S11 closes and the charging current is solely determined by the calibrated emitter resistance.
To compensate for the temperature coefficient of the transistor, the base voltage of V1212 is supplied via transistor V1214.
This also has the advantage of reducing the load on the TIME/DIV potentiometer R9.
This transistor, in turn, has its base controlled by preset potentiometer R1232 when TIME/DIV switch S10 is in one of the positions .5 s/div ... .5 ms/div. This provides a fine adjustment for the timing circuit in the slower sweep speeds. In these positions the preset potentiometer R1232 provides an additional measure of control over the base voltage of V1212. In the positions of S10 when C1207 is not in circuit, the diode V1218 is blocked and the preset control R1232 is inoperative.

The discharge circuit for the capacitors C1204 and C1207 consists of resistor R1219 and transistor V1213.
This switching transistor is driven by the sweep gating logic via a number of diodes. Diodes V1207 and V1208 form an AND-gate for positive logic; V1209 and V1211 adapt the level to control transistor V1213.
The resulting sawtooth voltage is taken from two transistors V1219 and V1221 in a kind of Darlington pair configuration.
C1209 improves the transfer of faster sawtooth signals at the expense of the input impedance which need not to be that high then. The sawtooth voltage amplitude is approx. 5 V. This sawtooth voltage is then fed to the X-final amplifier.

3.2.9.2. Hold-off circuit

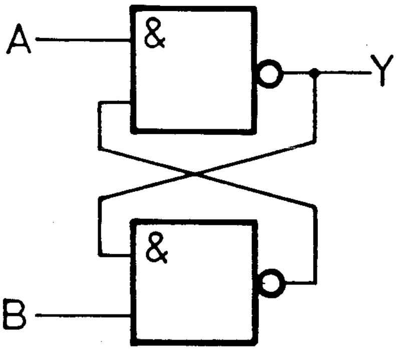
The hold-off circuit prevents the sweep gating logic from responding to trigger pulses before the time-base capacitor has fully discharged. The sawtooth output from the Darlington pair V1219 and V1221 is applied to the base of emitter follower V1223.
The switching transistor V1217 switches the hold-off capacitor C1208 in circuit, parallel to C1206, according to the position of the TIME/DIV switch S10, in a similar manner to that described for the time-base integrator timing capacitor. Capacitor C1206 is always in circuit irrespective of the TIME/DIV switch position.
Charging current for the hold-off capacitors flows via transistor V1223. When V1223 cuts off the discharge current flows through R1228 and hold-off control R12. This current is adjustable to change the hold-off time.
The voltage across hold-off capacitors C1206 or C1206 + C1208 follows the sawtooth voltage fairly fast in positive going direction via emitter follower V1223. When a certain value is reached, integrated Schmitt-trigger D1201 reacts and the end of the sweep is initiated.
This is followed by a hold-off period in which the voltage across the hold-off capacitor decreases fairly slowly until the lower switching level of the Schmitt trigger is reached. The system can now be triggered again. In the mean-time also the time-base integrator timing capacitor C1204 or C1204 + C1207 has reached its quiescent state. The output (point 6) of D1201 is low during the hold-off time, at any other moment this output is high.

3.2.9.3. *Sweep gating logic*

The sweep gating logic which consists of TTL logic circuit is controlled by the following signals:

- The trigger signals supplied by the trigger comparator.
- The voltage supplied by the hold-off circuit.
- The voltage supplied by the auto circuit via the hold-off circuit.

The TTL circuit D1201 contains four 2-input NAND-gates with Schmitt-trigger properties.
D1202 contains four normal 2-input NAND-gates and D1203 contains three normal 3-input NAND-gates.
With the aid of the various gates two flip-flops are formed.



A	B	Y
0	0	1
0	1	1
1	0	0
1	1	Old situation

Fig. 3.16. Flip-flop symbol

Y is A, if B is 0
Y is 1, if A is 0

The circuit is set by A is 0 (when B is 1) and reset by B = 0 (when A is 1).
See relation diagram of the sweep gating logic in the AC or DC mode.

1 The incoming trigger signal from the trigger comparator switches the Schmitt-trigger output (D1201, point 11) to zero after a positive going edge has exceeded the upper switching level (+1.7 V) of this Schmitt-trigger.

2 After this, the first flip-flop output (D1202), point 3) is set to the logic 1-state.

3 If the negative going edge of the incoming trigger signal drops below the lower switching level (+0.9 V) of the Schmitt-trigger, the output (D1201 point 11) switches to logic 1 level again.

4, 5, 6 The logic 1 state of the first flip-flop and the output signal of the Schmitt-trigger allows the setting of the second flip-flop output (D1203, point 6) to the zero state by means of the NAND output (D1202, point 11).

7 The output signal of the second flip-flop is applied to switching transistor V1213 via an OR-gate which consists of E1216, V1207 and V1208. This signal causes the sweep to start.

8 The end of the sweep is reached when the signal across the hold-off capacitor C1206 exceeds the upper switching level (+1.7 V) of the hold-off Schmitt-trigger. The output of this Schmitt-trigger switches then to zero.

9 Both flip-flops are now reset. Switching transistor V1213 starts conducting and time-base capacitor C1204 will discharge.

10 The voltage across the hold-off capacitor C1206 decreases slowly until the lower switching level (+0.9 V) of the Schmitt-trigger is reached.

11 This is the end of the hold-off period. The output (D1201, point 6) of the hold-off Schmitt-trigger rises to 1 again and the system can be triggered again.

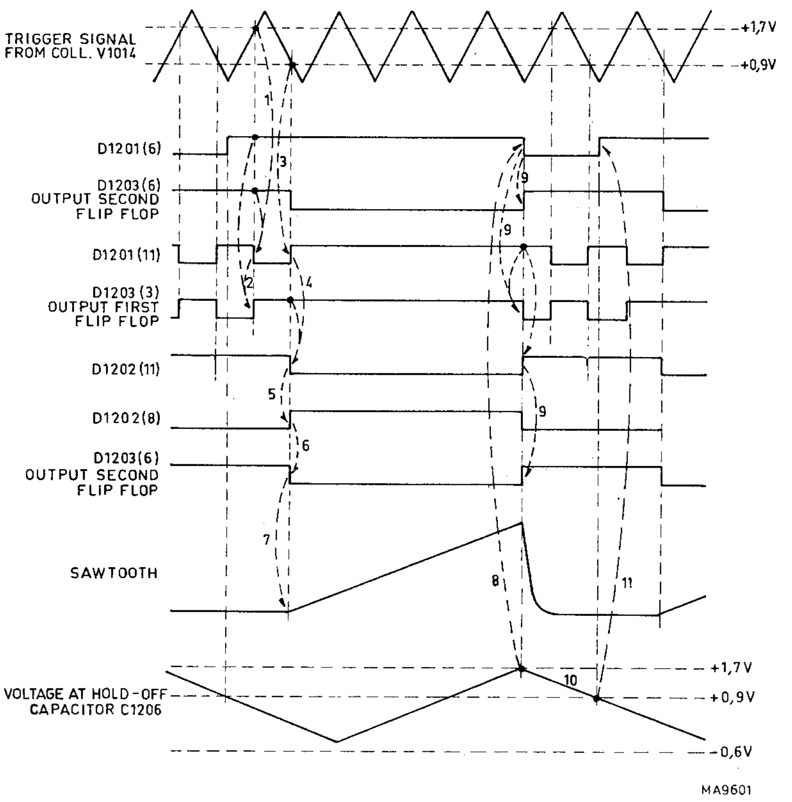

TRIGGER SIGNAL FROM COLL. V1014
+1,7V
+0,9V
D1201(6)
D1203(6) OUTPUT SECOND FLIP FLOP
D1201(11)
D1203(3) OUTPUT FIRST FLIP FLOP
D1202(11)
D1202(8)
D1203(6) OUTPUT SECOND FLIP FLOP
SAWTOOTH
VOLTAGE AT HOLD-OFF CAPACITOR C1206
+1,7V
+0,9V
-0,6V
1
2
3
4
5
6
7
8
9
10
11
MA9601

Fig. 3.17. Time relation diagram of the sweep-gating logic in the AC or DC mode

3.2.9.4. Auto sweep circuit

In the absence of a trigger signal the auto sweep circuit will provide a display on the screen. Transistor V1203 senses the state of the output of the second flip-flop, this is the output of the sweep gating logic. When this point reaches the logic zero level, transistor V1203 starts conducting enabling C1202 to discharge. Transistors V1204 and V1206 are then turned off. The collector of V1206 lies on –0.7 V potential and the relevant gate of D1201 is then blocked. This means that output D1201 (3) is at logic 1 level (+5 V).

In the absence of a trigger signal, the output D1203 (6) of the sweep gating logic remains a logic 1 level (+5 V) and transistor V1203 remains turned-off. The voltage across capacitor C1202 increases until approximately 100 msec., transistor V1204 starts conducting and causes transistor V1206 to conduct. The collector of V1206 rises to approximately +5 V and the relevant gate of D1201 opens. The hold-off signal on point 6 of D1201 now can reach via gate D1201 (3) and the OR-gate, the switching transistor V1213. The loop is then closed and the time base generator is in the free runing mode.

3.2.9.5. X-final amplifier

Transistor V1407 is driven by either the time-base generator via diodes V1411 and V1409 when R1406 is kept at +12 V level via TIME/DIV switch S10 (in all the TIME/DIV positions of this switch), or the amplifier stage V1404 when R1407 is kept at +12 V level via TIME/DIV switch S10 (in position X DEFL), or the horizontal DAC via output socket X25 point 4.

Transistor V1404 receives its input signal from D1001 point 8 of the trigger amplifier.

This signal is derived from one of the sources, channel A, channel B, analyzer (i.e. trigger-word pulse) or an external source, depending on the setting of the X deflection selector switch S16.

The final X amplifier consists of two amplifier stages in parallel (one for each deflection plate).

Only one half is described.

The actual amplifier is the cascode circuit with transistors V1414 and V1416.

The resistors R1428 and R1429 are feedback resistors. The bias current for the amplifier is supplied by transistor V1413. The average voltage on the deflection plate is kept at +26 V by means of zener diodes V1424 and V1426. Capacitor C1413 improves the h.f. response.

This final stage is supplied from the +180 V and –180 V because the X plates of the C.R.T.are mechanically displaced such that they are less sensitive than the Y plates.

The cascode amplifier stages are controlled via the transistors V1406 and V1407.

3.2.10. Cathode-ray tube circuit

The cathode-ray tube circuit comprises the C.R.T. itself and the brightness, focus, astigmatism, geometry and trace rotation controls and the beam blanking amplifier. A block diagram of the C.R.T. circuit is given in Fig. 3.18.

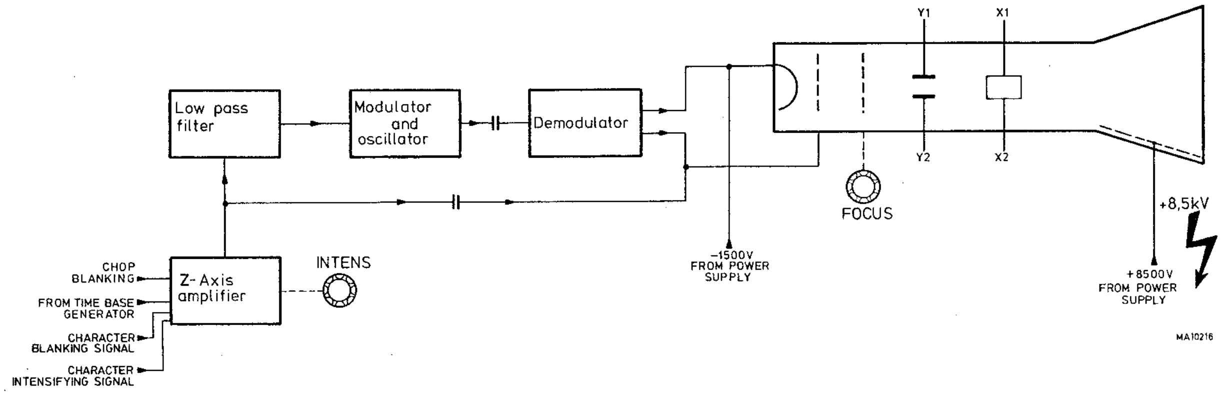

Y1
X1
Low pass filter
Modulator and oscillator
Demodulator
Y2
X2
FOCUS
+8,5kV
CHOP BLANKING
FROM TIME BASE GENERATOR
CHARACTER BLANKING SIGNAL
CHARACTER INTENSIFYING SIGNAL
Z-Axis amplifier
INTENS
−1500V FROM POWER SUPPLY
+8500V FROM POWER SUPPLY
MA10216

Fig. 3.18. Cathode-ray tube circuitry

3.2.10.1.C.R.T. controls

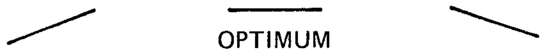
By means of the INTENS potentiometer R1, the brightness of the display can be continuously controlled. The display can be focused by means of the FOCUS potentiometer R6. Both INTENS and FOCUS controls are front panel controls.

The C.R.T. circuitry also has preset potentiometers for trace rotation, astigmatism and geometry.

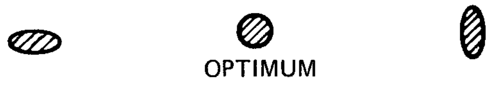
The FOCUS control R6 forms a part of a voltage diviser network across the 1.5 kV output of the power supply. The slider of this potentiometer is connected direct to the focus, grid G3.

TRACE ROTATION is achieved by means of the trace rotation coil L1501. This coil mounted inside the mu-metal screen, provides a magnetic field for rotational control of the entire scan. The degree and direction of rotation is determined by the setting of front panel potentiometer R10 (screwdriver operated). The slider of R10 is connected to the bases of the complementary transistors V1521 and V1522.

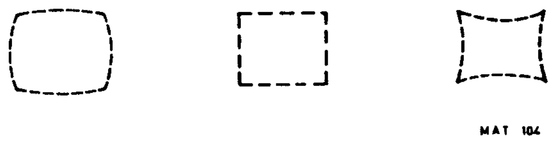
The trace rotation coil L1501 is supplied by these transistors.



With the ASTIGMATISM control R1543, the form of the spot can be corrected by adjusting the voltage on the grids G2 and G4.



With the GEOMETRY control R1549 the barrel and pin-cushion distortion is corrected by adjusting the voltage on the grid G7.



3.2.10.2.Beam blanking amplifier

The beam blanking amplifier receives three input signals. The first one is a signal, originated in the time-base generator and is applied to the amplifier to unblank the trace during the sweep.

The second one is supplied by the channel switch to blank the trace during switching from channel to channel in the chop mode.

The third one is a character intensifying signal and is delivered by the horizontal latch D2079.

The INTENS potentiometer R1 determines the amount of input current fed to the amplifier.

In all the time/div. positions of the TIME/DIV switch S10, the anode of diode V1202 is kept at approx. +12 V, resulting in a logic 1 level at input 1 of NAND D1203.

The output point 12 of this NAND is now at logic 1 level when either input 2 or input 3 is low. In other words only during a sweep.

In the X DEFL position of the TIME/DIV switch S10, input 1 of NAND D1203 is at a logic 0 level, and in that case the output point 12 of this NAND is steady at logic 1 level. This output signal is inverted by a NAND and fed via diodes V1501 and V1503 of the beam blanking amplifier.
The chop mode blanking signal from the channel switch is fed to transistor V1506 via R1502. The inverted and amplified signal is applied to diode V1508.
Both signals are joined together at the base of transistor V1514 (point A in figure 3.19). This is the virtual earth point of a shunt feedback amplifier.

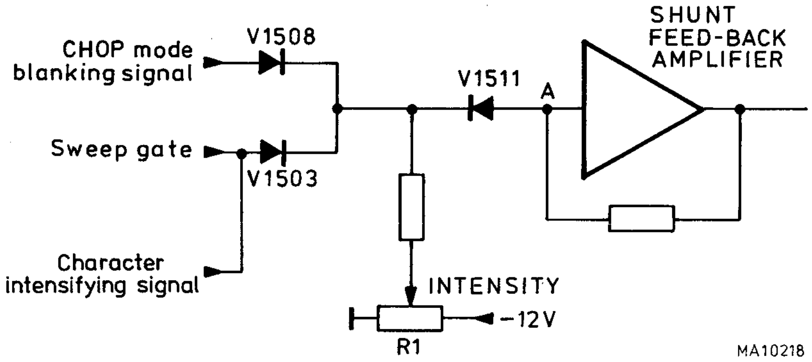

SHUNT FEED-BACK AMPLIFIER
CHOP mode blanking signal
V1508
V1511
A
Sweep gate
V1503
Character intensifying signal
INTENSITY
-12V
R1
MA10218

Fig. 3.19. Shunt feed-back amplifier

Assume that V1503 and V1508 are turned-off by applying a logic zero to both inputs.
Then the output voltage of the amplifier can be varied with the aid of INTENS potentiometer R1. The light on the screen is variable then e.g. during a sweep or in the X deflection mode. A logic 1 on either one or both inputs of the diodes V1503 and V1508 turns V1511 off. The C.R.T. is then blank e.g. between sweeps or during the sweep when there is channel switching in the chop mode.

The blanking signal is amplified in the stage with transistors V1512, V1513 and V1514. At the output of this amplifier the a.c. and d.c. components of the blanking signal are guided along different paths. The a.c. path runs straight to the Wehnelt cylinder of the C.R.T. via capacitor C1512.
A d.c. signal is fed to the emitter of transistor V1517 via a low-pass filter R1528/C1508/R1527. Transistor V1517 constitutes a multivibrator together with transistor V1516. The a.c. voltage on the collector of V1517 has a peak-to-peak value which depends on the voltage fed to the emitter of V1516 by the shunt feed-back amplifier.

The a.c. voltage supplied by multivibrator V1516/V1517 is applied to a peak detector. This peak detector rectifies this a.c. voltage.

The reason for the a.c. and d.c. paths is to isolate the cathode and Wehnelt cylinder, which are on a —1.5 kV potential, from the other circuits. The a.c. component of the blanking signal is transmitted directly to the high-voltage part via blocking capacitor C1512, which is a high voltage capacitor. The d.c. signal, however, is converted into a a.c. voltage and then transmitted to the high-voltage part, via capacitor C1509, after which it is rectified by means of diode V1519.
The dark level can be adjusted with the aid of potentiometer R1534 in the emitter circuit of transistor V1517 in the d.c. amplifier.

3.2.11. Power supply

The power supply comprises a mains transformer and rectifier, a DC to AC converter regulator and a transformer and output voltage rectifier.
The power supply also incorporates a circuit for the graticule illumination.

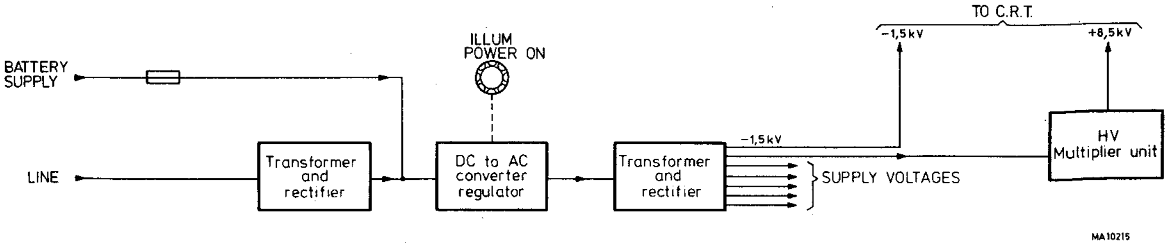

TO C.R.T.
-1,5kV
+8,5kV
ILLUM POWER ON
BATTERY SUPPLY
LINE
Transformer and rectifier
DC to AC converter regulator
Transformer and rectifier
-1,5kV
HV Multiplier unit
SUPPLY VOLTAGES
MA10215

Fig. 3.20. Power supply

The line part of the PM 3540 power supply is double insulated and meets IEC 348 SAFETY CLASS II recommendations for metal-encased electrical equipment. This eliminates the need for a 3-wire power cord with earth connection.
The converter together with the primary of the converter transformer is electrically floating in relation to mass. Therefore also the 24 V d.c. supply is floating.

3.2.11.1. Mains transformer

An incoming mains voltage is fed via the thermal fuse (F101) and the voltage selector S18 to the appropriate primary taps on the mains transformer T101. Transformer T101 has three primary windings which can be combined by means of voltage adapter S18. This combination allows the instrument to be used with mains voltages of 110 V, 127 V, 220 V and 240 V.

The voltage on the secondary windings of this transformer is full-wave rectified. The resulting negative d.c. voltage (approx. 24 V) across electrolytic capacitor C203, or alternatively a negative d.c. voltage on the rear panel DC POWER IN input socket X7, is applied to the voltage stabilizer and converter.

3.2.11.2. Converter and stabilized power supply

The converter is a square-wave generator operating at a frequency of approx. 18 kHz and driven by the d.c. voltage across the electrolytic capacitor C203.
A basic diagram of the converter is shown in Fig. 3.21.

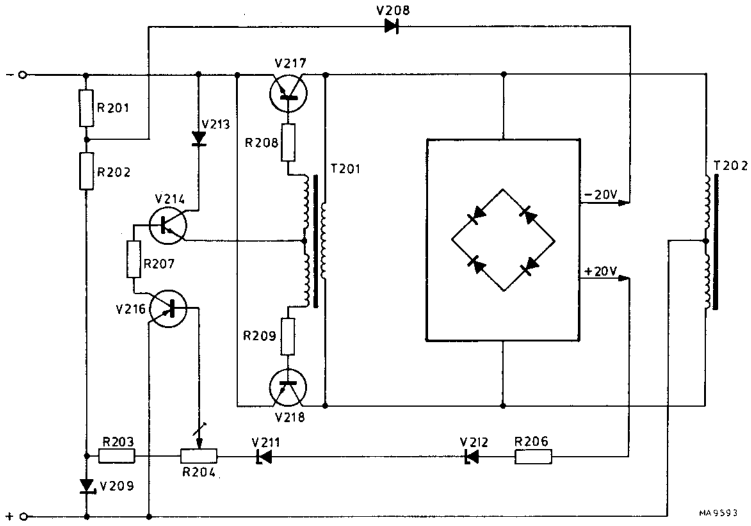


Fig. 3.21. Basic diagram of the converter

In the converter, transistors V217 and V218 function as switches and regulators and alternately connect the negative supply voltage to either end of the primary of T201/T202. Assume that transistor V217 has a slightly higher current gain than V218, then the positive voltage from the feedback winding quickly drives transistor V217 into saturation. The current in the top half of the primary of T201/T202 increases linearly at a rate determined by the inductance of the primary. This current increase continues until the iron in transformer coil T201 is saturated.
Then the magnetic lines of flux stop changing and consequently no voltage is induced in the feedback winding. When its base drive ceases, the transistor is cut off.
This reverses the polarity of the feedback voltage and transistor V218 is turned hard on. The bottom half of the primary then passes on increasing current until the core is saturated in the opposite direction.
The subsequent absence of feedback voltage inititates the switching back to V217 and the cycle starts again.

The regulation works as follows. When an input voltage is applied to the converter, the negative voltage across Zener diode V209 turns transistor V216 fully on, as there is no positive voltage from temperature compensation stabistors V211 and V212.
Then a bias current flows via transistor V216 through resistor R207, through the base-emitter junction of transistor V214 (operating as a diode since diode V213 interrupts the collector circuit) and from base to emitter of both transistors V217 and V218.

As there is then an a.c. voltage across the primary of T201/T202, diodes V222 and V223 produce a positive d.c. voltage of +20 V across capacitor C209. This voltage reduces the current through transistors V216 and V214 sufficiently to limit the drive to transistors V217 and V218 and produce the desired output level. The setting of potentiometer R204 determines the value of the regulated output voltage. Possible differences from the set output voltage are fed back via the temperature compensation stabistors V211 and V212 to transistor V216 so that the drive of transistors V217 and V218 is adapted so as to compensate for the differences. This also applies to mains voltage fluctuations.

After rectifying and smoothing, the secondary voltages +5 V, –5 V, +12 V, –12 V, +38 V, +180 V, –180 V, –1500 V and post acceleration voltage +8500 V are obtained. The voltage quintupler which supplies the +8500 V cannot be repaired and must be replaced when it breaks down.
T202 contains a separate secondary winding for the heater voltage for the C.R.T.
All supply voltages except the +8500 V and the –1500 V can be continuously short-circuited without damage to the components. Resistor R202 limits the collector current when the output is short-circuited and the switching action is stopped, thereby holding the dissipated power in transistors V217 and V218 at a safe level. Thus, the power supply of the oscilloscope is fully protected against short-circuits. A short-circuit is indicated either by a squeaking noise coming from the power supply or by the pilot lamp B1, which indicates the ON state of the oscilloscope, failing to light up.
If supplied by an external d.c. voltage, the instrument is protected against overloads and wrong polarity by internal fuse F201 and diode V206.

3.2.11.3. Illumination circuit

The graticule of the C.R.T. can be illuminated by means of the bulbs E1. The intensity can be varied with the aid of ILLUM potentiometer R11 which ontrols the collector current (which is the current through the bulbs) of transistor V207. The illumination circuit is not short-circuit proof.

3.2.12. Calibration unit

The calibrator circuit consists of transistors V1602 and V1603, which are configured as a stable multivibrator such as used in the channel switch. Good shape of the wave-form is obtained by a constant current supplied by transistor V1602 which will flow in turn through the left hand or right hand transistor. The amplitude is 1,2 V or 6 div in the 20 mV/div attenuator positions. (The straight through position of the attenuator.)
Potentiometer R1607 allows accurate adjustment of the amplitude of the calibrator output voltage. This square-wave output voltage is taken from the collector of transistor V1603 and fed to socket X1. This is the front panel CAL terminal.
The calibrator output signal can be used for probe compensation and/or checking the vertical deflection accuracy.

3.3. CHECKING AND ADJUSTING

3.3.1. General information

The following information provides the complete checking and adjusting procedure for the PM 3540 logic-scope. As some of the circuits are interdependent, the given order of checking is advised. The procedures are, therefore, presented in a sequence that is best suited to this order. Prior to checking and adjusting a particular circuit, care must be taken to ensure the accuracy of all associated circuits.

Only skilled personnel aware of the hazards involved should perform those adjustments which necessitate the removal of covers from an instrument that is connected to the mains supply. In all other circumstances, covers should remain fitted as long as the instrument is live (see also chapter 2, "DIRECTIONS FOR USE").

The tolerances stated in the checking and adjusting procedures apply only to instruments which are completely set up, and may differ from the data given in the specification chapter i.e. 1.2. CHARACTERISTICS.
All adjusting elements have been listed in the headings of the various sections. Allow a warming-up time of 30 minutes before checking and adjusting.

3.3.1.1. Test equipment and tools required

For a complete checking and adjusting procedure, you will need the tools and test equipment listed in the following table.

TEST EQUIPMENT

Description of the test instrument	*Specification of the test instrument*	*Suitable test instrument*	*Usage*
Digital multimeter.	AC/DC instrument, accuracy within 0,1 %.	Philips PM 2526 or equivalent.	C.R.T. circuit. Trouble shooting.
Time-mark generator.	Providing markers of 0,55 to 0,1 μs, accuracy within 0,5 %.	–	Time-base timing checks.
T.V. pattern generator or T.V. source.	Providing frame and line sync pulse output. Ampl. at least 40 mV.	Philips PM 5504 or equivalent.	Time-base, T.V. triggering.
Squarewave generator or amplitude calibrator.	Providing output voltages variable from 10 mV to 12 V (accuracy within 0,5 %), frequency range 2 KHz ... 1 MHz, rise time $\leqslant$ 3 ns.	–	Attenuator response, vertical gain and response checks.
Sinewave generator.	Providing output voltages variable from 10 mV to 10 V frequency range 20 Hz ... 35 MHz.	Philips PM 5145 suitable for most purposes.	Vertical amplifier bandwidth and triggering checks. Trouble shooting.
Monitor oscilloscope and analyzer or combination.	0 ... 35 MHz bandwidth	Philips PM 3540 or equivalent.	Trouble shooting. Adjusting.
Amp.-meter.	Movinr-iron meter.	–	Mains current consumption.
Variable mains transformer.	Well insulated for safe checking.	Philips 2422 529 00005.	Trouble shooting.
Probe 10x attenuation.	Suitable for input capacies of 20 pF to 30 pF.	Philips PM 8925 or equivalent.	Trouble shooting.
Logic pulser.	Provides in-circuit stimulus.	See Fig. 3.25.	Trouble shooting.
Logic tracer.	To indicate the in-circuit stimulus.	See Fig. 3.25.	Trouble shooting.
Trimming tool kit.	Low capacitance trimming tool.	Philips. See Fig. 3.35.	Adjusting and maintenance.

3.3.2. Power supply

3.3.2.1. Mains current

- Check that the mains voltage adapter (S18) has been set to the **local** mains voltage and connect the instrument to such a voltage.
- Switch the oscilloscope on and check that the pilot lamp on the front panel lights up.
- Check that the current consumption does not exceed 200 mA at 220 V local mains and 400 mA at 117 V local mains. (Measured with a moving iron meter.)

3.3.2.2. Supply voltages (R204)

- Check that the voltage across capacitor C224 is +12 V, + or −0,25 V; if necessary readjust potentiometer R204 (Fig. 3.22.).
- Check the supply voltages in accordance with the following table:

Voltage across	*Required value*	*Max. allowable ripple*
C227 (Fig. 3.22.)	+5 V, ± 0,2 V	⩽ 2 mVp-p
C224 (Fig. 3.22.)	+12 V, ± 0,25 V	⩽ 4 mVp-p
C229 (Fig. 3.22.)	−12 V, ± 0,25 V	⩽ 4 mVp-p
C222 (Fig. 3.22.)	+38 V, ± 2 V	⩽ 40 Vp-p
C231 (Fig. 3.22.)	−180 V, ± 9 V	⩽ 1 Vp-p
C221 (Fig. 3.22.)	+180 V, ± 9 V	⩽ 1 Vp-p
C211 (Fig. 3.22.)	6,3 V, ± 0,6 V	

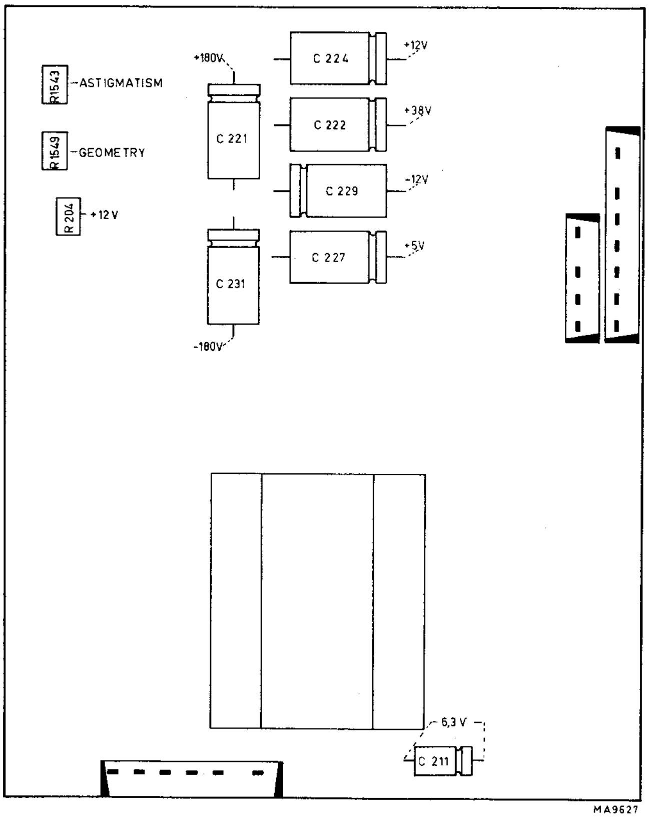


Fig. 3.22. Adjusting and checking the power supply.

- Vary the a.c. voltage to which the instrument is connected + or −10 % of the nominal voltage.
- Check that the supply voltages do not vary more than ± 2 % and that the ripple voltages do not exceed the values mentioned in the table above.

3.3.3. Cathode-ray tube circuit

3.3.3.1. Brilliance (R1534)

- Depress push button A of the display mode switch S1.
- Set TIME/DIV switch S10 to position EXT X DEFL.
- Depress push button EXT of the trigger source selector switch S16.
- Set A POSITION potentiometer R2 and X POSITION potentiometer R4 to their mid-positions.
- Set INTENS potentiometer R1 to 90° from its left hand stop.
- Adjust potentiometer R1534 (Fig. 3.24.) until spot just disappears.

3.3.3.2. Trace rotation (R10)

- Depress push button AUTO of the trigger mode switch S2.
- Set TIME/DIV switch S10 to 0,1 ms/div.
- Depress push button A of the display mode switch S1.
- Depress push button A of the trigger source selector switch S16.
- Depress the input coupling switch S13 (0).
- Center the time-base line using A POSITION potentiometer R1.
- Check that the time-base line runs exactly in parallel with the horizontal lines of the graticule. If necessary, readjust front panel TRACE ROTATION potentiometer R10.

3.3.3.3. Focus and astigmatism (R1543)

- Depress push button A of the display mode switch S1.
- Depress push button A of the trigger source selector switch S16.
- Depress the input coupling switch S12 (AC).
- Releast the input coupling switch S13 (0).
- Set A AMPL/DIV switch S6 to 0,1 V/div and A AMPL/DIV potentiometer R7 to CAL.
- Set TIME/DIV switch S10 to 50 μs/div and TIME/DIV potentiometer R9 to CAL.
- Apply a sine-wave voltage of approx. 600 mVp-p, 10 kHz, to the A input socket X2.
- Set INTENS potentiometer R1 for normal brightness.

Use an insulated screw-driver.

- Adjust FOCUS potentiometer R6 and astigmatism potentiometer R1543 for a sharp and well-defined trace (Fig. 3.22.).

3.3.3.4. Geometry (R1549)

- Set the controls as in the previous section.
- Set A AMPL/DIV switch S6 to 5 mV/div and A AMPL/DIV potentiometer R7 to CAL.
- Apply a sine-wave voltage of approx. 600 mVp-p, 10 kHz, to the A input socket X2.

Use an insulated screw-driver.

- Check that the displayed vertical lines are as straight as possible. If necessary readjust potentiometer R1549 (Fig. 3.22.).

3.3.4. Y-amplifier balance

3.3.4.1. General information

The adjustments of the vertical amplifier channels A and B are identical. The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.

3.3.4.2. D.C. balance (R504, R604)

- Depress push button A (B) of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Depress the input coupling switch S13 (S15) (0).
- Set AMPL/DIV potentiometer R7 (R8) to CAL.
- Centre the trace using A (B) POSITION potentiometer R2 (R3).

- Check that the trace does not jump if AMPL/DIV switch S6 (S8) is switched from 10 mV/div to 20 mV/div. If necessary, adjust potentiometer R504 (R604) for minimum jumps (Fig. 3.24.).
- Repeat the measurement for channel B.

3.3.4.3. Gain balance (R514, R614)

- Depress push button A (B) of the display mode switch S1.
- Depress the input coupling switch S13 (S15) 0.
- Check that the trace does not move when the AMPL/DIV potentiometer R7 (R8) is rotated. If necessary readjust R514 (R614) (Fig. 3.24.).
- Repeat the measurement for channel B.

3.3.4.4. Normal/invert balance channel B (R647)

- Depress push button B of the display mode switch S1.
- Depress the input coupling switch S15 (0).
- Check that the trace does not jump when PULL TO INVERT B switch S4 is switched between normal and invert. If necessary readjust R647 (Fig. 3.24.).

3.3.4.5. Shift balance (R547, R647)

- Depress push button A (B) of the display mode switch S1.
- Depress push button A (B) of the trigger source selector switch S16.
- Depress the input coupling switch S12 (S14) (AC).
- Release the input coupling switch S13 (S15) (0).
- Set the AMPL/DIV switch S6 (S8) to 20 mV/div and AMPL/DIV potentiometer R7 (R8) to CAL.
- Set the TIME/DIV switch S10 to 50 μs/div and TIME/DIV potentiometer R9 to CAL.
- Apply a sine-wave voltage of 480 mVp-p, 10 kHz to the A (B) input socket.
- Check if the extremes of the sine-wave can be displayed distortion free on the screen by rotating the POSITION potentiometer R2 (R3).
  If necessary readjust potentiometer R547 (R647) (see Fig. 3.24.).
- Repeat the measurement for channel B.

3.3.5. Trigger balance (R356, R358, R361)

- Depress push button A of the display mode switch S1.
- Set X MAGN switch S5 to position X1.
- Set TIME/DIV switch S10 to 0.1 ms/div and TIME/DIV potentiometer R9 to CAL.
- Depress push button AUTO of the trigger mode switch S2.
- Set X POSITION potentiometer R4 so that the time base line starts at the most left graticule line.
- Set TIME/DIV switch S10 to DEFL.
- Depress push button EXT of the trigger source selector switch S16.
- Check that the spot is in the center of the screen; tol. 1 div.
- Depress push button A of the trigger source selector switch S16.
- Depress push button DC of the trigger mode switch S2.
- Check that the spot is in the center of the screen.
  If necessary readjust potentiometer R356 (Fig. 3.23).
- Depress push button B of the trigger source selector switch S16.
- Check that the spot is in the center of the screen.
  If necessary readjust potentiometer R361 (Fig. 3.23.).
- Depress both A and B push buttons (composite) of the trigger source selector switch S16.
- Shift the spot to the central horizontal graticule line using A POSITION potentiometer R2.
- CHECK that the spot is in the center of the screen.
  If necessary readjust potentiometer R358 (Fig. 3.23.).

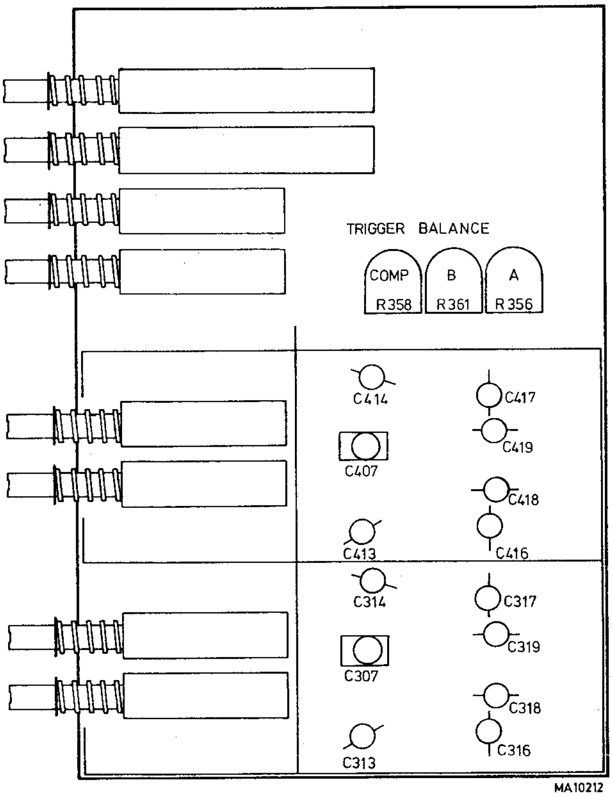


Fig. 3.23. Adjusting elements attenuator board

3.3.6. Time coefficients (R1417, R1419, R1232)

- Depress push button A of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Set X MAGN switch S5 to position X1.
- Set A AMPL/DIV switch S6 to 20 mV/div.
- Release the input coupling switch S13 (0).
- Depress push button A of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 2 μs/div and TIME/DIV potentiometer R9 to CAL.
- Apply a time marker voltage with repetition time of 2 μs and an amplitude of 80 mVp-p to the A input socket X2.
- Check that the central 8 cycles occupy 8 divisions.
  If necessary readjust potentiometer R1417 (Fig. 3.24.).
- Pull X MAGN switch S5 to position X10.
- Change the repetition time of the applied input signal to 0.2 μs.
- Check that the central 8 cycles occupy 8 divisions.
  If necessary readjust potentiometer R1419 (Fig. 3.24.).
- Check that the trace can be shifted over 100 divisions with the aid of X-POSITION potentiometer R4.
- Push X MAGN switch S5 to position X1.
- Set TIME/DIV switch S10 to 5 ms/div.
- Change the repetition time of the applied input signal to 5 ms.
- Check that the central 8 cycles occupy 8 divisions.
  If necessary readjust potentiometer R1232 (Fig. 3.24.).
- Check all the other positions of the TIME/DIV switch S10. The repetition time of the applied input signal should correspond to the position of the TIME/DIVISION switch S10.
  The central 8 cycles should always occupy 8 divisions: tolerance ± 1 subdivision (2 subdivisions with X MAGN switch S5 to position x10).
- Check that in all the positions of the TIME/DIV switch S10 the time-base length is at least 10 divisions.
- Check the control range of the TIME/DIV potentiometer R9 in the position 0.1 ms/div of the TIME/DIV switch S10. This should be 1 : $\geqslant$ 2.5.

3.3.7. Vertical amplifiers

3.3.7.1. General information

The adjustments of the vertical amplifier channels A and B are identical. The knobs, sockets and adjusting elements of channel B are shown in brackets after those of channel A.

3.3.7.2. Deflection sensitivity (gain)

The adjustments of the vertical amplifier sensitivity must follow the specified sequence.

Channel B	X1	Gain	(R848)
Channel A	X1	Gain	(R543)
Channel B	X10	Gain	(R621)
Channel A	X10	Gain	(R521)

Deflection sensitivity X1 (R848, R543)

- Depress push button B (A) of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Depress push button B (A) of the trigger source selector switch S16.
- Set AMPL/DIV potentiometer R8 (R7) to CAL.
- Release input coupling switch S14 (S12) (DC).
- Release input coupling switch S15 (S13) (0).
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Set AMPL/DIV switch S8 (S6) to 20 mV/div.
- Apply a square-wave voltage of 120 mV, frequency approx. 2 kHz, to the B (A) input socket.
- Check that the signal occupies 6 divisions.
  If necessary readjust potentiometer R848 (R543) (Fig. 3.24.).
- Repeat the measurement for channel A.

Deflection sensitivity X10 (R621, R521)

- Depress push button B (A) of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Depress push button B (A) of the trigger source selector switch S16.
- Set AMPL/DIV potentiometer R8 (R7) to CAL.
- Release input coupling switch S14 (S12) (DC).
- Release input coupling switch S15 (S13) (0).
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Set AMPL/DIV switch S8 (S6) to 2 mV/div.
- Apply a square-wave voltage of 12 mVp-p, frequency approx. 2 kHz, to the B (A) input socket.
- Check that the signal occupies 6 divisions.
  If necessary readjust R621 (R521) (Fig. 3.24).

Repeat the measurement for channel A.

3.3.7.3. Input attenuators

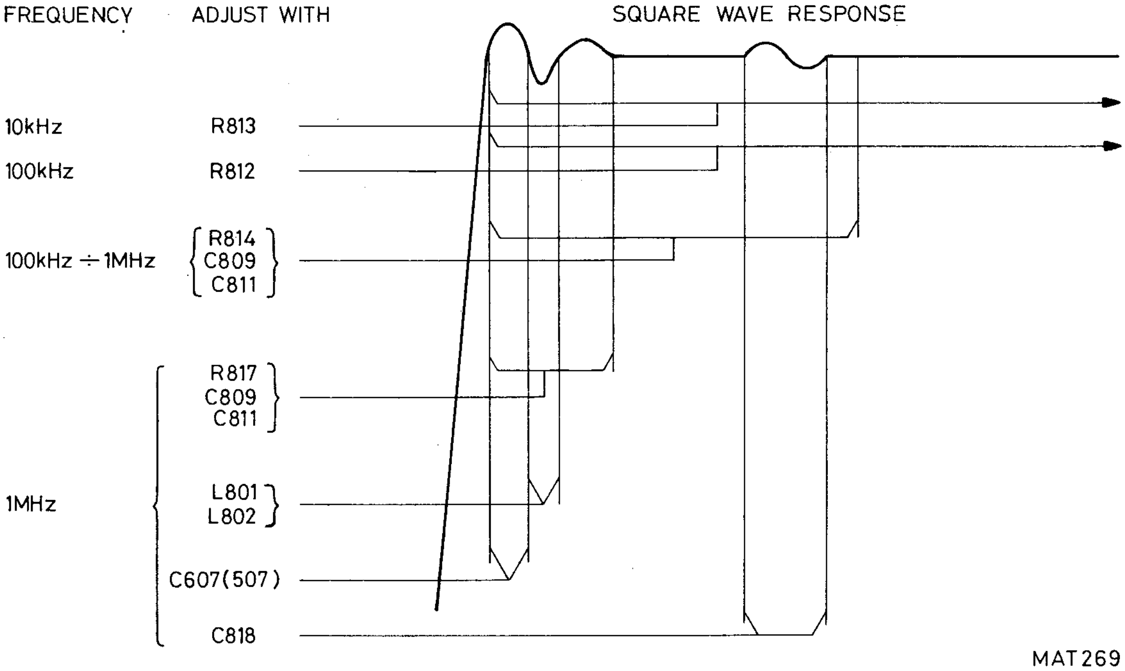
- Depress push button A (B) of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Depress push button A (B) of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 0,2 ms and the TIME/DIV potentiometer R9 to CAL.
- Release input coupling switch S12 (S14) (DC).
- Release input coupling switch S13 (S15) (0).
- Set AMPL/DIV potentiometer R7 (R8) to CAL.
- Apply a square-wave voltage with an amplitude as indicated in the following table, a repetition rate of approx. 2 kHz and a rise time ≤ 100 ns, to the A (B) input socket.
- Check that no overshoot is visible (max. pulse top errors 2 %), and check that the trace height is 6 divisions ± 3 % (1 subdivision).

S6 (S8) ampl. to	Input signal	Adjust with
20 mV	120 mV	C307 (C407)
50 mV	0,3 V	C313 (C413)
0,1 V	0,6 V	C314 (C414)
0,2 V	1,2 V	C316+C318 (C416+C418)
2 V	12 V	C317+C319 (C417+C419)

- Repeat the measurement for channel B.

3.3.7.4. Square-wave response final amplifier

- Depress push button B of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Depress push button B of the trigger source selector switch S16.
- Push NORMAL/INVERT switch S4 to position NORMAL.
- Set B AMPL/DIV switch S8 to 20 mV/div and B AMPL/DIV potentiometer R8 to CAL.
- Apply a square-wave voltage of approx. 120 mVp-p, with rise time ⩽ 3 ns, to the B input socket. The pulse repetition should be in accordance with the table below.
- Check the square-wave response, pulse top errors may not exceed 1 subdivision.
- Check that the rise time does not exceed 14 ns.



* L801 and L802 should be operated simultaneously and in the same direction and by the same amount. If necessary repeat above adjustments until the best response is obtained.

- Check and readjust the square-wave response according to the table below.

Channel	Ampl/div	Input signal	Trace height	Rep.rate	Time/div	Adj. with	Max. error
B	2 mV/div	12 mV	6 div.	1 MHz	0,2 µs	C602	1 subdivision
A	20 mV/div	120 mV	6 div.	1 MHz	0,2 µs	C508	1 subdivision
A	2 mV/div	12 mV	6 div.	1 MHz	0,2 µs	C502	1 subdivision

3.3.7.5. Cross talk (R813)

- Depress push button CHOP of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Depress push button B of the trigger source selector switch S16.
- Push NORMAL/INVERT switch S4 to position NORMAL.
- Set A and B AMPL/DIV switches S6 and S8 to 20 mV/div and the AMPL/DIV potentiometer R7 and R8 to CAL.
- Set the TIME/DIV switch S10 to 0,5 ms/div and the TIME/DIV potentiometer R9 to CAL.
- Depress the input coupling switch S13 (0).
- Apply a square-wave voltage of 120 mVp-p, rise time ⩽ 3 ns and a repetition rate of approx. 10 kHz to the B input socket.
- Adjust potentiometer R813 (Fig. 3.24.) for minimum cross talk between channels.

3.3.7.6. Bandwidth check of channel A (B)

- Depress push button A (B) of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.

- Depress push button A (B) of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 0,1 ms/div and the TIME/DIV potentiometer R9 to CAL.
- Set AMPL/DIV switch S6 (S8) to 2 mV/div and AMPL/DIV potentiometer R7 (R8) to CAL.
- Release input coupling switch S12 (S14) (DC).
- Release input coupling switch S13 (S15) (0).
- Apply a sine-wave signal of 12 mVp-p, frequency approx. 100 kHz to the A (B) input socket.
- Increase the frequency of the input signal to 35 MHz, the amplitude of the signal must remain 12 mV.
- Check that the trace height is at least 4,2 divisions at input frequency of 35 MHz.

Repeat the measurement for channel B.

3.3.8. Triggering

3.3.8.1. Trigger slope (R1014)

- Depress push button A of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Depress push button A of the trigger source selector switch S16.
- Depress input coupling switch S13 (0).
- Set LEVEL potentiometer R5 to its midposition.
- Check with a multimeter that the DC output voltage of the trigger amplifier (collector of V1014) does not change if SLOPE push button S3 is switched between + and –.
  If necessary readjust potentiometer R1014 (Fig. 3.24.).
- Set AMPL/DIV switch S6 to 20 mV/div and AMPL/DIV potentiometer R7 to CAL.
- Releast input coupling switch S12 to (DC).
- Release input coupling switch S13 (0).
- Apply a sine-wave signal of 120 mVp-p, frequency approx. 2 kHz, to the A input socket.
- Set TIME/DIV switch S10 to 0,2 ms/div.
- Release SLOPE switch S3 to the + position and check that the trace starts with a positive going edge.
- Depress SLOPE switch S3 to the – position and check that the trace starts with a negative going edge.

3.3.8.2. Trigger sensitivity (R1041)

- Set the controls as on the previous section.
- Apply a sine-wave signal of 120 mVp-p, frequency approx. 2 kHz to the A input socket.
- Find the lowest possible input signal at which it is still possible to obtain a triggered trace with the aid of LEVEL potentiometer R5 and potentiometer R1041 (Fig. 3.24.).

3.3.8.3. Trigger level internal DC

- Depress push button A of the display mode switch S1.
- Depress push button DC of the trigger mode selector switch S2.
- Depress push button A of the trigger source selector switch S16.
- Apply a sine-wave signal for a trace height equivalent of 16 divisions to the A input socket.
- Check that the starting point of the sine-wave can be shifted across 16 divisions with the aid of LEVEL potentiometer R5.
- Enlarge the vertical deflection to 24 divisions and check that the level range of R5 does not exceed 24 divisions.

3.3.8.4. Trigger level auto

- Depress push button A of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Depress push button A of the trigger source selector switch S16.
- Release input coupling switch S13 (0).
- Apply a sine-wave voltage at a frequency of approx. 100 Hz for 6 divisions trace height to the A input socket.
- Check that the starting point of the sine-wave can be shifted across approx. 3 divisions with the aid of LEVEL potentiometer R5.

3.3.8.5. *Trigger level external*

- Depress push button A of the display mode switch S1.
- Depress push button AC of the trigger mode switch S2.
- Depress push button EXT of the trigger source selector switch S16.
- Release input coupling switch S12 (DC).
- Release input coupling switch S13 (0).
- Set A AMPL/DIV switch S6 to 1 V/div and A AMPL/DIV potentiometer R7 to CAL.
- Set TIME/DIV switch S10 to 0,2 ms/div. and TIME/DIV potentiometer R9 to CAL.
- Apply a sine-wave signal of 8 Vp-p, frequency approx. 2 kHz to the A and EXT input sockets.
- Check that the starting point of the sine-wave can be shifted across the entire amplitude of the signal with the aid of LEVEL potentiometer R5.

3.3.8.6. *Trigger sensitivities*

- Check the trigger sensitivity in accordance with the table below or better.

Trigger source S16	Trigger mode S2	+/– S3	Trace height or ampl.	Signal to	Freq.	Shape	Ampl. input voltage
A	Auto	+	1 div.	X2 (YA)	100 Hz	Sine	20 mVp-p
A	Auto		1 div.	X2 (YA)	10 kHz	Sine	20 mVp-p
A	Auto		1 div.	X2 (YA)	35 MHz	Sine	28 mVp-p
A	AC		1 div.	X2 (YA)	20 Hz	Sine	20 mVp-p
A	AC		1 div.	X2 (YA)	35 MHz	Sine	28 mVp-p
A	DC		1 div.	X2 (YA)	35 MHz	Sine	28 mVp-p
B	DC		1 div.	X3 (YB)	20 Hz	Sine	20 mVp-p
B	DC		1 div.	X3 (YB)	35 MHz	Sine	28 mVp-p
A+B	DC		1 div.	X3 (YB)	35 MHz	Sine	28 mVp-p
A+B	DC			X2 (YA)	± 2 kHz	Square*	± 20 mVp-p
(compl)				X3 (YB)	± 2 kHz	Sine*	± 20 mVp-p
(S1 in ALT)							
B	TV	+	0,7 div. Sync. pulse	X3 (YB)		+ Video	14 mVp-p Sync. pulse
B	TV	–	0,7 div. Sync. pulse	X3 (YB)		– Video	14 mVp-p Sync. pulse
B	TV	–	± 2 div. Sync. pulse	X3 (YB)		– Video	± 40 mVp-p Sync. pulse
EXT	DC		0,2 Volt	X4 (EXT)	20 Hz	Sine	0,2 Vp-p
					35 MHz	Sine	0,2 Vp-p
EXT 10	DC		2 Volt	X4 (EXT)	20 Hz	Sine	2 Vp-p
					35 MHz	Sine	2 Vp-p

* Originating from different sources.

- Set LEVEL potentiometer R5 as required.
- Set TIME/DIV switch S10 so that a reasonable number of sine-waves is displayed.
- Set A and B AMPL/DIV switches S6 and S8 to 20 mV/div. and the A and B AMPL/DIV potentiometers R7 and R8 to CAL.

3.3.8.7. *Triggering on the line frequency*

- Depress push button A of the display mode switch S1.
- Depress push button AUTO of the trigger mode switch S2.
- Depress push button B of the trigger source selector switch S16.
- Set TIME/DIV switch S10 to 5 ms/div and TIME/DIV potentiometer R9 to CAL.
- Set A AMPL/DIV switch S6 to 20 mV/div and A AMPL/DIV potentiometer R7 to CAL.
- Release input coupling switch S12 (DC).

- Release input coupling switch S13 (0).
- Apply a signal of approx. 10 mVp-p at the mains frequency to the A input socket.
- The trace is not triggered.
- Depress push button LINE of the trigger source selector switch S16 and check that the trace is triggered.

3.3.9. X-Deflection

3.3.9.1. Sensitivity

- Set TIME/DIV switch S10 to X DEFL.
- Depress push button EXT of the trigger source selector switch S16.
- Apply a sine wave voltage of 4 Vp-p frequency approx. 10 kHz, to the EXT input socket.
- Check that the trace length is 8 divisions ± 0,8 division.

3.3.9.2. Frequency response

- Set TIME/DIV switch S10 to X DEFL.
- Depress push button EXT of the trigger source selector switch S16.
- Apply a sine-wave voltage of 4 Vp-p (trace length 8 divisions), frequency approx. 10 kHz, to the EXT input socket.
- Increase the frequency to 1 MHz.
- Check that the trace length is at least 5,6 divisions.

3.3.9.3. X Deflection with a line signal

- Set TIME/DIV switch S10 to X DEFL.
- Depress push button LINE of the trigger source selector switch S16.
- Check that the trace length is 8 divisions ± 1 division.

3.3.9.4. Horizontal sensitivity via input A

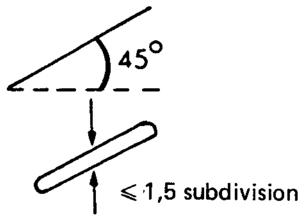
- Set A AMPL/DIV switch S6 to 20 mV/div and A AMPL/DIV potentiometer R7 to CAL.
- Depress push button B of display mode switch S1.
- Set TIME/DIV switch S10 to X DEFL.
- Depress push button A of the trigger source selector switch S16.
- Apply a sine wave voltage of 120 mVp-p, frequency approx. 2 kHz, to the A input socket.
- Check that the trace length is 6 divisions ± 0,6 division.

3.3.9.5. Horizontal sensitivity via input B

- Set B AMPL/DIV switch S8 to 20 mV/div and B AMPL/DIV potentiometer R8 to CAL.
- Depress push button A of display mode switch S1.
- Set TIME/DIV switch S10 to X DEFL.
- Depress push button B of the trigger source selector switch S16.
- Apply a sine wave voltage of 120 mVp-p, frequency approximately 2 kHz, to the B input socket.
- Check that the trace length is 6 divisions ± 0,6 division.

3.3.9.6. Phase difference between X and Y channels

- Input signal and control settings as in the previous section.
- Depress push button B of the display mode switch S1.
- Check that the line is displayed under an angle of 45°.
- Increase the frequency to 100 kHz.
- Check that the phase error does not exceed 3° division).



3.3.10. Calibration voltage (R1607)

- Check that the voltage on the CAL output socket is 1,2 V ± 1 %. If necessary readjust potentiometer R1607 (Fig. 3.24.).

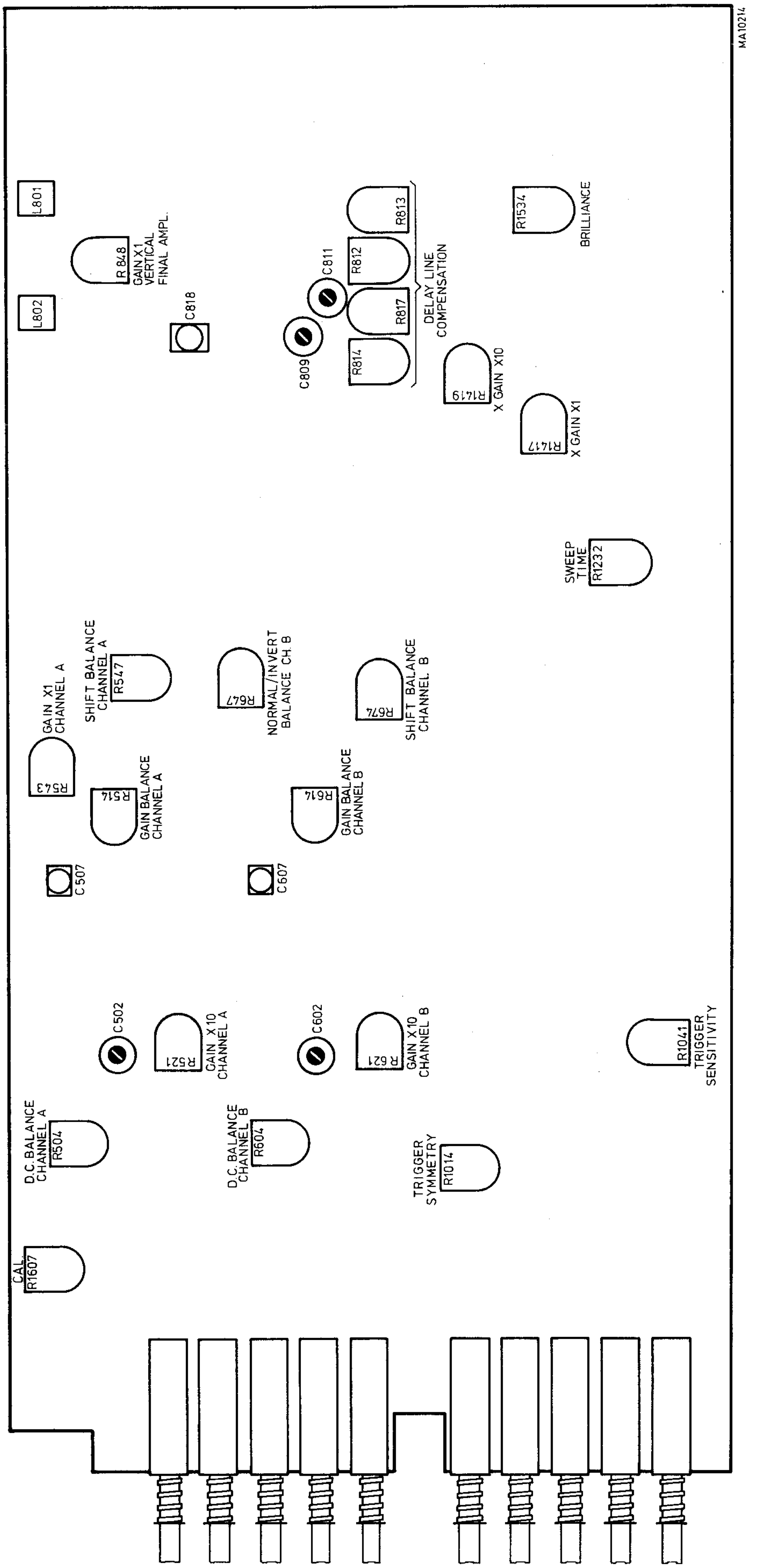

MA10214
L801
L802
R848
GAIN X1
VERTICAL
FINAL AMPL.
C818
C809
C811
R813
R812
R817
R814
DELAY LINE
COMPENSATION
R1534
BRILLIANCE
R1419
X GAIN X10
R1417
X GAIN X1
SWEEP
TIME
R1232
GAIN X1
CHANNEL A
R543
SHIFT BALANCE
CHANNEL A
R547
R647
NORMAL/INVERT
BALANCE CH.B
R674
SHIFT BALANCE
CHANNEL B
R514
GAIN BALANCE
CHANNEL A
R614
GAIN BALANCE
CHANNEL B
C507
C607
C502
R521
GAIN X10
CHANNEL A
C602
R621
GAIN X10
CHANNEL B
R1041
TRIGGER
SENSITIVITY
D.C. BALANCE
CHANNEL A
R504
D.C. BALANCE
CHANNEL B
R604
TRIGGER
SYMMETRY
R1014
CAL.
R1607

Fig. 3.24. Adjusting elements amplifier board

3.3.11. L.S. Analyzer adjustments

3.3.11.1. Micro-processor board (Fig. 3.44.)

This board has only two calibration points:

- R2087, vertical shift in the analyzer mode, this adjustment potentiometer is accessible from the outside of the instrument (see Fig. 2.2.).
- R2024, to adjust the SYSCLK signal at 50 ns, tolerance + or – 5 ns.

3.3.11.2. Digital-to-analoga convertor board (Fig. 3.45)

This board has only one calibration point:

- R2130, to expand or contract the displayed format.

3.4. INFORMATION TO ASSIST IN FAULT-FINDING

GENERAL

This chapter is to assist in fault-finding in the oscilloscope circuitry in the micro-processor circuits and other circuits which are under micro-processor control.

3.4.1. Mains transformer data

The available unloaded voltage tappings and the number of turns per winding are listed in the circuit diagram (Fig. 3.53) in the form of a table.

3.4.2. Voltages and waveforms in the oscilloscope part of the instrument

The d.v. voltage levels at the electrodes of the transistors and the voltage waveforms in the time-base generator are shown at the relevant points on the circuit diagram (Fig.3.53).
The logic-scope under test must be set in the following way to measure the voltage wave-forms as shown in Fig. 3.53.

- Select the OSC mode.
- X-POSITION potentiometer R4 at mid-range.
- A-POSITION potentiometer R2 at mid-range.
- LEVEL potentiometer R5 at mid-range.
- SLOPE switch in position "+".
- TRIGGER source selector switch S16 in position "A".
- A and AUTO push-buttons S1A and S2A depressed.
- A AMPL/DIV switch S6 to 1 V/div. and potentiometer R7 to CAL.
- TIME/DIV switch S10 to 0,2 ms/div., potentiometer R9 to CAL and X MAGN switch S5 to x1.
- Input signal on A input socket X2: 2,5 kHz sine-wave voltage ofr 8 div. deflection.

3.4.3. Measurements in the analyzer part of the instrument

The PM 3540 is provided with a self test program consisting of several tests. These tests are non-selectable and selectable.
The non-selectable tests are carried-out automatically every time the power is switched on (power-up test).

The selectable tests can be executed as mentioned in para 3.4.5. "Service selftest routine".

3.4.3.1. Power-up test

Every time the instrument is switched-on, the micro-processor executes the power-up test, which consists of:

- PROM test (i.e. a check-sum test)
- Scratch-pad RAM test (i.e. a write-read test).

Normally the display on the c.r.t. appears approximately 10 s after switching-on.
If no display, or only one dot appears, one of the posibilities is that the micro-processor remains in the PROM test. The micro-processor is then continuously checking the sum of stored information in the EPROM's. If the display shows an address, the instrument is looping in the RAM test. The micro-processor is continuously checking the address which delivers the faulty data.

3.4.3.2. Oscilloscope checking of micro-processor bus signals

The 8085 micro-processor (D2059) is provided with the following busses:

- Address bus
- Data bus
- Control bus

In general, if signals on these bus lines are checked with an oscilloscope, a very unstable display will be the result.
This is due to the fact that these signals vary with time in a rather unpredictable way.
If anyhow a stable display of signals from one of these busses is obtained, this may be an indication that the micro-processor runs in a small program loop.
This phenomena is used when finding faults in the power-up test.

3.4.3.2. *Oscilloscope checking of micro-processor bus signals*

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3.4.4. Information about trouble shooting equipment (see also 3.3.1.1.)

- Though most of the test measurements can be carried out with a 2-channel oscilloscope, use of a 4-channel oscilloscope (e.g. PM 3244 or PM 3264) or an analyzer (e.g. PM 3540) is recommended.
- Logic pulser, used to check simple in-circuit functions of integrated circuits.
- Logic indicator probe.
- Current tracer probe, to detect and to trace short circuit current on p.c. boards.

Use of digital logic trouble shooting instruments

Connect a pulser probe to an input of a logic circuit.
Check the function of the circuit by connecting the indicator probe alternately to the input and the output of a circuit (see Fig. 3.25.). Always compare output with respect to input.

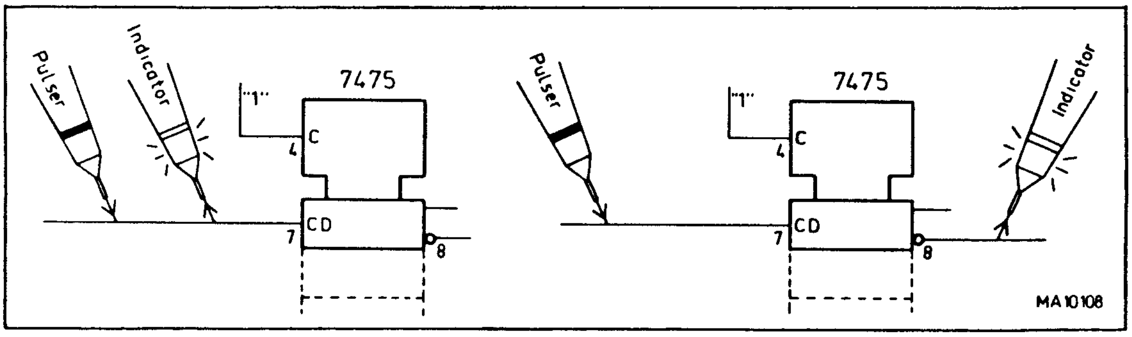


Fig. 3.25. Use of logic pulser and indicator probes

Remarks

In case of a defect it is always possible to apply to the world wide PHILIPS Service Organization.
When the instrument is to be sent to a PHILIPS Service Workshop for repair, the following points should be observed:

- Attach a label with your name and address to the instrument.
- Give a complete description of the faults found, or the service required.
- Use the original packing, or, if this is no longer available, carefully pack the instrument in a wooden crate or box.
- Send the instrument to the address obtained after consultation with the local PHILIPS Organization.

3.4.5. Service selftest routine

The PM 3540 has an integral program that enables a selftest routine of eight tests to be used as an aid in isolating functional faults and consists of a number of test modules that are sequentially activated. The program is selected by pressing STORE TRIG and STORE REF pushbuttons simultaneously which also initiates test 1, to enter test 2 the start button must be pressed and repeated to enter tests 3 and 4.
When the start button is pressed again the test loop through 8 is entered and the test numbers will be displayed sequentially, this does not mean that the tests have been completed successfully but that the user now has the opportunity to select any of the tests by pressing the start button when the required number is displayed, the selected part of the program will then run until the start button is pressed again when the test loop will be re-entered at the leaving point, the test sequence is indicated on the test flow chart, Fig. 3.26.
When a test is successful (measured by the Micro-processor) the string "TEST OK" will be displayed, if negative "TEST FAILS" (this applies to tests 4, 5, 6, 7 and 8 only) the program start conditions should then be checked. The circuit may now be checked, it is possible to use the units own oscilloscope because the test program will remain active when the PM 3540 is switched to the oscilloscope mode.

Settings

- Delay pushbutton ON
- No external clock
- External triggerqualifier OFF
- NO signal applied to external bus.

Leaving the service routine is achieved by pressing the pushbuttons STORE REF and 0/- simultaneously. The main program is started with the same default value for the variables as with a power up reset.
All the settings of the analyzer are lost when entering the service routine.

NOTE: In case of a fault, it is recommended to complete the eight tests so to optimize your diagnosis.

3.4.5.1. Summary of tests

Test 1 : Test of horizontal and vertical Digital to Analog Converter
Test 2 : Same as test 1 with other values
Test 3 : Test of character counter
Test 4 : Test of character generator
Test 5 : Test disabling Data Input by μProcessor
Test 6 : Test start data input controlled by μProcessor
Test 7 : Address counter test of data input memory
Test 8 : Delay counter test and stop data input

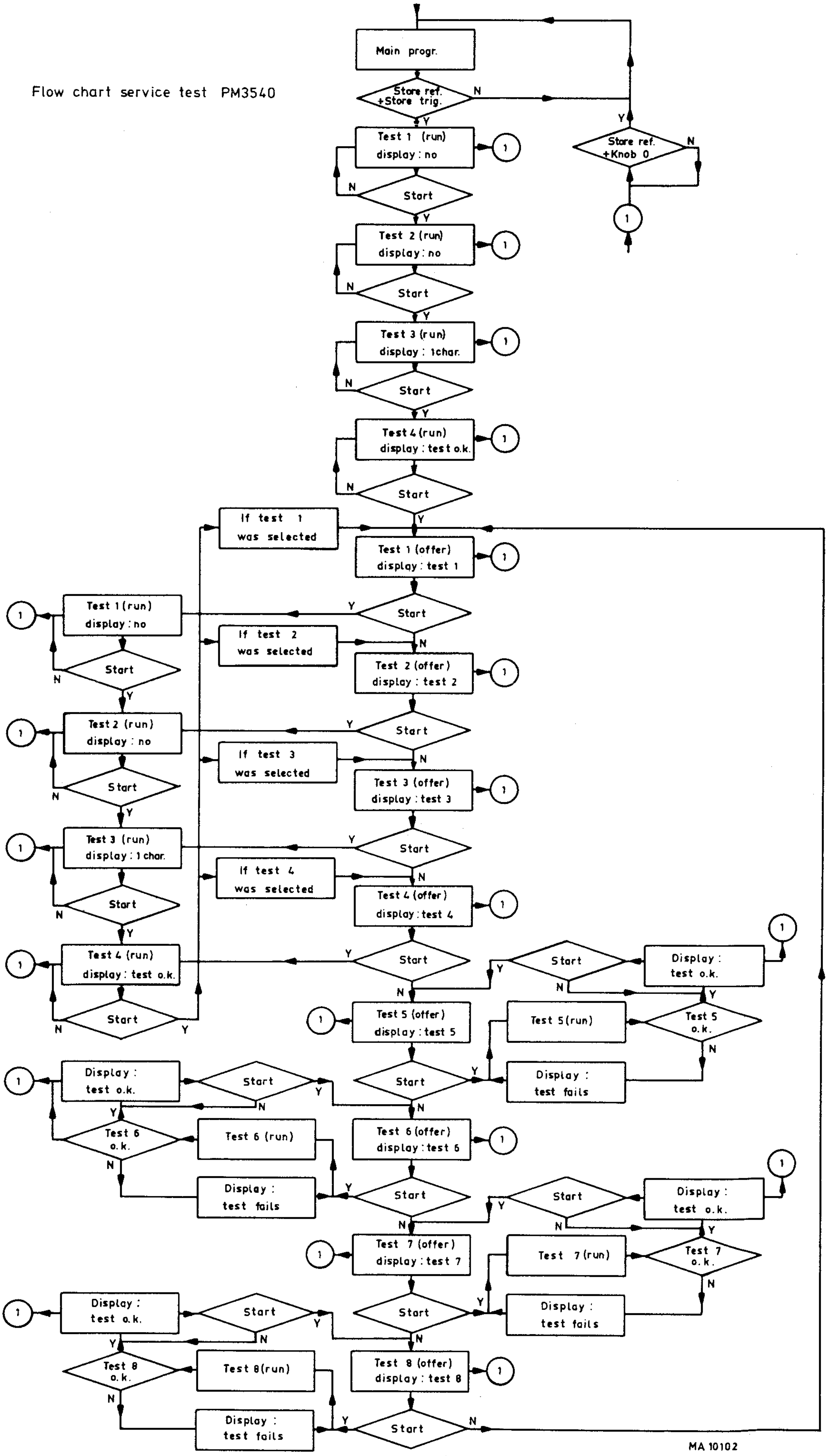
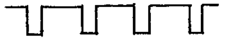
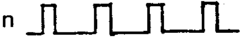

Flow chart service test PM3540
Main progr.
Store ref. +Store trig.
N
Y
Store ref. +Knob 0
Y
N
1
Test 1 (run) display : no
Start
Test 2 (run) display : no
Start
Test 3 (run) display : 1char.
Start
Test 4 (run) display : test o.k.
Start
If test 1 was selected
Test 1 (offer) display : test 1
Start
If test 2 was selected
Test 2 (offer) display : test 2
Start
If test 3 was selected
Test 3 (offer) display : test 3
Start
If test 4 was selected
Test 4 (offer) display : test 4
Start
Test 1 (run) display : no
Start
Test 2 (run) display : no
Start
Test 3 (run) display : 1 char.
Start
Test 4 (run) display : test o.k.
Start
Display : test o.k.
Start
Test 5 (run)
Test 5 o.k.
Display : test fails
Test 5 (offer) display : test 5
Start
Display : test o.k.
Start
Test 6 o.k.
Test 6 (run)
Display : test fails
Test 6 (offer) display : test 6
Start
Display : test o.k.
Start
Test 7 (run)
Test 7 o.k.
Display : test fails
Test 7 (offer) display : test 7
Start
Display : test o.k.
Start
Test 8 o.k.
Test 8 (run)
Display : test fails
Test 8 (offer) display : test 8
Start
Y
N
1
MA 10102

Fig. 3.26. Flow chart of service selftest routine

3.4.5.2. *Description of the tests*

Settings for a successful execution of the tests:
- delay pushbutton must be on.
- no external clock.
- external triggerqualifier must be off and no signal applied to the external bus.

Test 1

This test loads the horizontal and vertical Digital to Analog Converter with a defined pattern. The horizontal DAC is loaded with the pulse train  , which can be checked at the output connector of the LSA unit X20 (pins 8 – 10 – 12 respectively).
The pulse train  has to be measured at X20 (pins 9–11) and X22.
The vertical DAC, is loaded with 01010 which can be checked on LSA unit X19 (pins 8–9–10–11–12 respectively).
During this test there is no C.R.T. display (the circuit under test is D2078 and D2079).

Test 2

This is the same test as test 1 but with inverted signals on the pins mentioned.

Test 3

In this test the counter which scans the column's and the rows of a character is running (D2072 and D2073). The counting can be checked on LSA unit on X19 and C20 (pins 1, 2 and 3 respectively).
A character will be displayed on the screen while the character counter is running indicating that D2076 and D2077 are also being tested. The character which will be displayed is the last character that was loaded in the character latch (D2074) before you entered test 3.
Coming from the main program it is the character which was on the last digit of the triggerword in the heading of the display.

Test 4

The character generator is tested on some different characters.
The character string "TEST O.K." must be displayed. The user has to check the faultfree performance of the test because the μProcessor system isn't able to do it.

Test 5

The start/stop flip-flop D2023 is stopped by a control signal from μProcessor ($\overline{\text{HLTDI}}$ which means HALT Data Input). The μProcessor checks if the flip-flop reacts and displays "TEST O.K." or "TESTS FAILS" depending on the result of the check. In case of a failing test the test is repeated to give the opportunity to measure some signals in the circuit under test. Otherwise there is only the display routine.

Test 6

The start/stop flip-flop is started by a control signal from μProcessor ($\overline{\text{STRDI}}$ which means Start Data Input) and the output from the flip-flop is checked. The execution of the test is the same as test 5.

Test 7

The address counter (D2014 and D2017) of the Data input memory, is incremented 64 times and the result is checked by μProcessor after each clock pulse.
The clock pulses are generated by the μProcessor by means of pulsing the $\overline{\text{CLDIM}}$ signal on D2036 (pins 1...6). The course of the test is again the same as test 5.

Test 8

During this test there must no no input clock present and DELAY pushbutton must be depressed.
The delay counter is loaded by μProcessor, by means of control signal DELAY, with 9999. After that the data input is enabled ($\overline{\text{STRDI}}$).
The delay counter is now decremented by clockpulses that are generated by changing the clockedge on D2029 input (pin 1) twice for each clockpulse.
The system must be disabled after 10000 clockpulses. This is checked at each clockpulse and "TEST O.K." or "TEST 8 FAILS" is displayed etc.
In this test it is also possible to check the external trigger qualifier circuit. Therefore it is necessary that no signal is applied to the external BNC bus.
The test must be entered with the pushbuttons EXT and DATA (= EXT. QUAL) both depressed. Now test 8 must fail until a High signal (a signal with a voltage greater than the adjusted threshold voltage) is applied on the EXT BNC bus.
In this way it is also posible to check the correct operation of the threshold voltage: Apply a voltage to a external trigger qualifier and check that test 8 remains failing until the threshold voltage is lower than the voltage applied to the external BNC bus.

3.5. DISMANTLING THE INSTRUMENT

3.5.1. General information

WARNING: This instrument must be disconnected from any voltage source before covers are removed.

This section describes the procedures necessary for the replacement of components during repair operations. All circuit boards removed from the unit should be adequately protected against damage and workshop practice of a high quality should be observed, during dismantling procedures a careful note must be made of any disconnected cables and plugs so that they may be correctly reconnected when the unit is reassembled.
Damage may result if the unit is switched on after a circuit board has been removed or if a circut board is removed within one minute of switching off.

3.5.2. Removal of instrument covers

The unit is protected by three covers: a front panel protection cover, a wrap round cover with carrying handle and a rear panel on which the mains input transformer is mounted.
To remove wrap round cover and rear panel first ensure that the front cover is in position.

Then proceed as follows:
- Push both pivot centre buttons of the carrying handle and hinge it clear of the front cover.
- Stand the unit on the front cover on a flat surface.
- Slacken the two coin slot screws located on the rear panel (Fig. 2.12.).
- Lift the rear panel and unplug the connector on power supply printed circuit board.
- Lift off the wrap round cover.
- For access to the front panel, stand the unit horizontally and snap off the front cover.

3.5.3. Removal of carrying handle

- Prise off centre knob from each pivot using a screwdriver (Fig. 2.12.) in one of the small slots in the side of the knobs.
- Remove the cross-slotted screws that are now accessible.
- Spring both arms slightly outwards and remove.
- Grip and arms are ordered separately (see list of mechanical parts), and a complete handle can be readily constructed by pushing the arms into the grip.

3.5.4. Removal of Bezel and contrast filter

- Take hold of the Bezel's bottom corners and gently pull it from the front panel (Fig. 2.15.).
- The contrast filter can be removed by pressing it gently out of the Bezel.

3.5.5. Removal of control knobs and text plate

- The AMP/DIV and TIME/DIV knobs can be removed after pulling off the small knobs and then uncrewing the hescagon nuts.
- The "X" position and "B" position knobs are removed by prising off the knob cap and undoing the slotted nut that is then accessible.
- The remaining small knobs can then be pulled off of the shafts.
- The earth terminal nut must then be removed.
- The text plate can be removed after the three hexagon nuts from the AMP/DIV and TIME/DIV switches have been unfastened.

3.5.6. Removal and replacement of the C.R.T. and the tube screen

- Remove unit covers and rear panel (section 3.5.2.).
- Remove Bezel and contrast filter (section 3.5.4.).
- Unplug connections on C.R.T. neck.
- Ease base socket off C.R.T.
- Slacken C.R.T. neckbrace.
- Unplug the trace rotation coil connector on the main amplifier board and pull cable and plug through the elongated hole in the centre frame.
- Withdraw the C.R.T. through the front panel until the E.H.T. connector is accessible.
- Remove the E.H.T. connector.
- Pass the C.R.T. right through the front panel taking care with the cable and plug of the trace rotation coil.
- The tube screen can now be removed by unfastening the two retaining screws on the rear panel.
- Installation is in reverse order, position the C.R.T. screen flush with the contrast filter.
- The torque applied to the screw of the brace around the C.R.T. neck must be between 0.4 and 0.6 Nm.

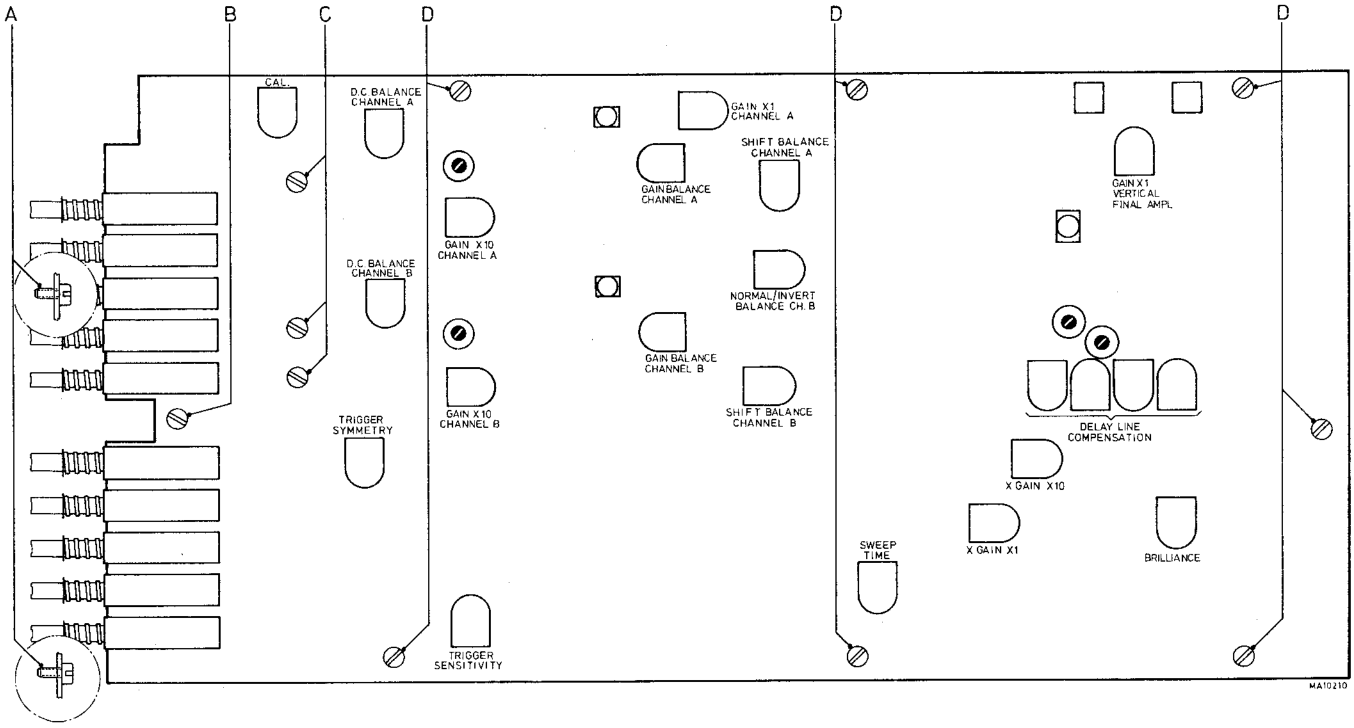

A
B
C
D
D
D
CAL.
D.C.BALANCE CHANNEL A
GAIN X1 CHANNEL A
SHIFT BALANCE CHANNEL A
GAINBALANCE CHANNEL A
GAIN X10 CHANNEL A
D.C.BALANCE CHANNEL B
NORMAL/INVERT BALANCE CH. B
GAIN BALANCE CHANNEL B
GAIN X10 CHANNEL B
SHIFT BALANCE CHANNEL B
TRIGGER SYMMETRY
GAIN X1 VERTICAL FINAL AMPL.
DELAY LINE COMPENSATION
X GAIN X10
X GAIN X1
SWEEP TIME
BRILLIANCE
TRIGGER SENSITIVITY
MA10210

Fig. 3.27. Removal of the amplifier board

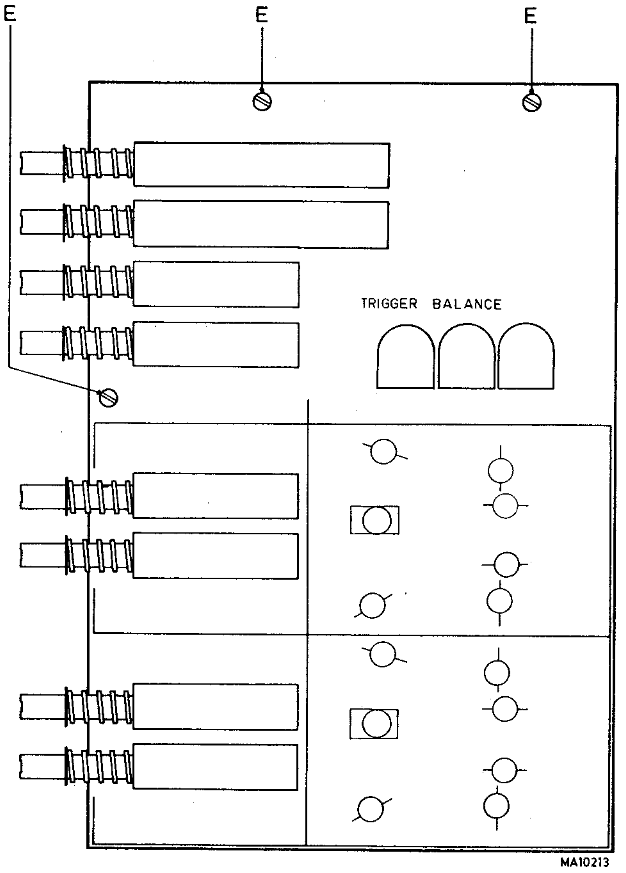

E
E
E
TRIGGER BALANCE
MA10213

Fig. 3.28. Removal of the attenuator board

3.5.7. Removing the front assembly

In order to gain access to parts on the AMPL/DIV switches, to replace trimmer capacitors or other components on the attenuator board, it is best to remove the front panel assembly as a whole in accordance with the following procedure.

- Remove the instrument covers in accordance with section.
- Remove the INTENS, FOCUS and ILLUM knobs by pulling them off the shaft.
- Remove the earthing terminal at the front.
- Remove the three screws A and B (Fig. 3.27.).
- Remove the three screws E that hold the attenuator board to the frame bar (Fig. 3.28.).
- Remove the three screws C (Fig. 3.27.).
- Make a note of the positions of the miniature socket connections on the amplifier board.
- Remove all plugs, miniature sockets, coaxial sockets and clamping terminals from unit and amplifier board.
- Remove the complete front assembly from the instrument: screening covers can then be removed to gain access to and remove parts.
- When the front panel assembly is reinstalled, make sure not to interchange the connections of the Y position controls. The connections are correct when trace shifts upwards if Y position control is rotated clockwise.

3.5.8. Removal of the main amplifier p.c. board

- Remove covers and rear panel (section 3.5.2.).
- Remove all plugs and leads, taking care to mark to faciliate reassembly.
- Remove the eleven retaining screws B, C and D (Fig. 3.27.).
- The main amplifier board can now be carefully lifted out of the instrument.

3.5.9. Replacing switches

- To replace the AMPL/DIV switches, first remove the front panel assembly (section 3.5.7.).
- To replace the TIME/DIV switch, first remove knobs and test plate (section 3.5.5.).
- If one of the push-button switches of the trigger source selector (A, B, EXT, LINE) or the input coupling switch (AC/DC 0) must be replaced, it is best to remove the front panel assembly (first section 3.5.7.). The defective switch is then replaced in accordance with the procedure described below.
- To replace one of the push-button switches of the vertical mode switch (A, ALT, CHOP, ADD, B) or the trigger mode switch (AUTO, AC, DC, TV., SLOPE), the amplifier board (section 3.5.8.) can be removed if so desired and the defective switch is then replaced as described below.

3.5.9.1. To remove a push-button switch mounted on a p.c. board

- Remove the printed circuitboard for replacing a switch in this unit.
- Straighten the 4 retaining lugs of the relevant switch as shown in Fig. 3.29.
- Break the body of the relevant switch by means of a pair of pliers and remove the pieces. The soldering pins are then accessible.
- Remove the soldering pins and clean the holes in the printed-wiring board (e.g. with a suction soldering iron or sucking copper litze-wire).
- Solder the new switch onto the printed-circuit board.
- Bend the 4 retaining lugs back to their original positions.

Note: The ALT switch is a dummy switch which can be replaced by a not self-releasing type.

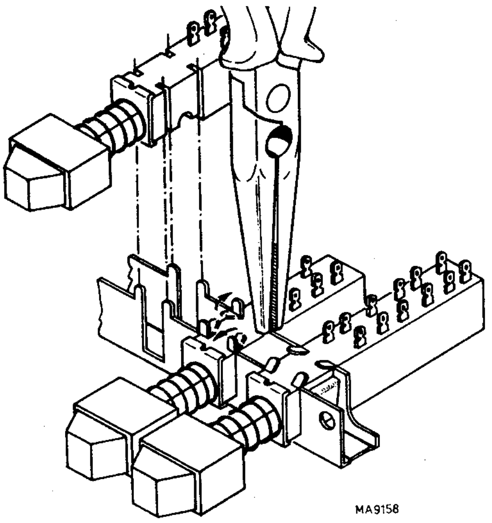


Fig. 3.29. Replacing a switch-segment

3.5.9.2. To remove a push-button switch, fitted to the front panel by means of clamping devices

- The Allen-key screws that secure the push-button set to the front panel must be removed (Fig. 3.30).
- Straighten the 4 retaining lugs of the relevant switch as shown in Fig. 3.29.
- Remount the new switch.
- Bend the four retaining lugs back to their original positions.

Note: Before a push-button set is refitted to the front panel, it is advisable to stick the two parts of the clamping device together by means of adhesive tape or non-hardening glue, in order to facilitate replacement, refer to Fig.

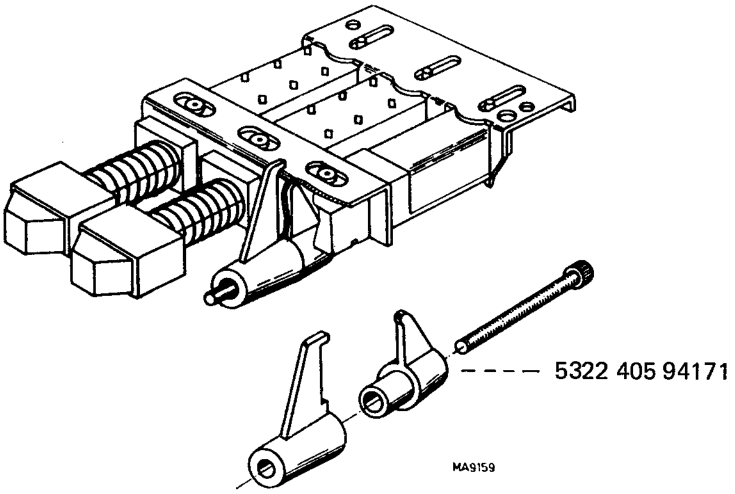


Fig. 3.30. Push-button set clamping device

3.5.10. Replacing the delay line unit

- Remove wrap round cover and rear panel (section 3.5.2.).
- The delay line is located under the main amplifier board and is fastened on to the inside of the side panel.
- If there is a fault in the delay line then the whole unit must be replaced.
- Replacement is selfevident but care must be taken when reconnecting. (Interchanging the connections results in a downwards movement of the trace when rotating the position control clockwise.)
- Before mounting the new unit it must be checked that the new delay line is housed as shown in Fig. 3.31.

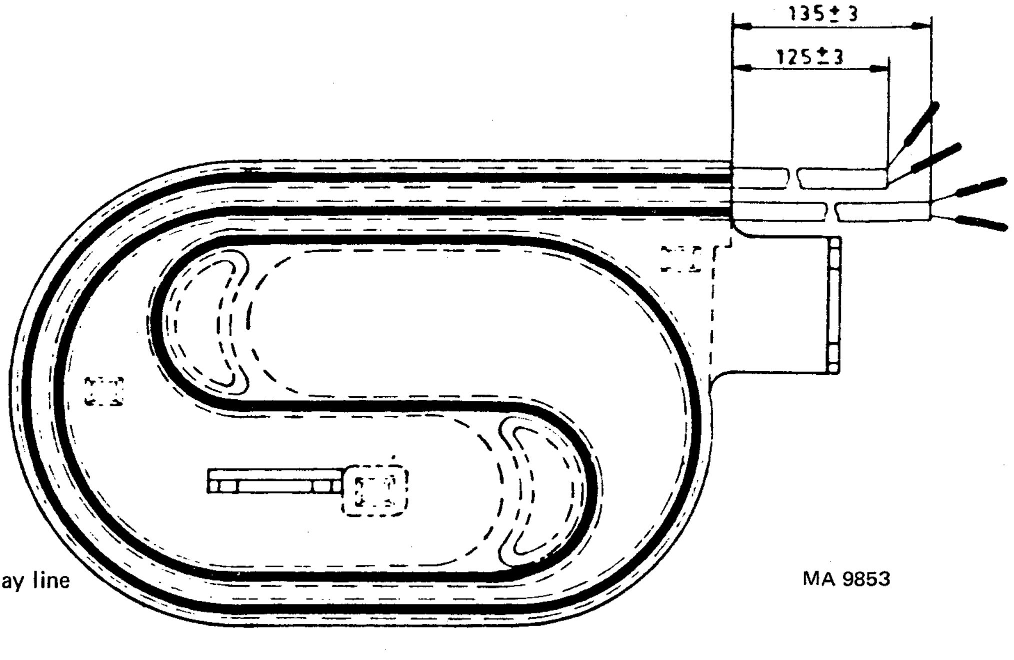


Fig. 3.31. Delay line

MA 9853

3.5.11. Removing the mains transformer

- Remove rear panel (section 3.5.2.).
- Remove the lid of the voltage selector compartment.
- Remove the lid of the transformer compartment.
- Lift the lid of the transformer compartment with the attached transformer at the same time sliding the cable from the voltage selector out of the slot in the transformer compartment.
- The transformer and thermal fuse are then accessible.

3.5.12. Replacing the thermal fuse

- Remove mains transformer (section 3.5.10.).
- Unsolder fuse terminals 1 and 2 (Fig. 2.13. & 2.11.).
- Only the fuse wire is replaced.
- Bend the housing of the fuse slightly outwards.
- Disengage the locking pin and pull out the wire.
- Push the new fuse wire into the housing until the locking pin snaps into the hole.
- The loop in the fuse wire must point to terminal 1.
- Solder the fuse wire to terminals 1 and 2.

3.5.13. Removal of power supply printed circuit board

- Remove wrap round cover and rear panel (section 3.5.2.).
- Ensure connections are unplugged.
- Unfasten the two slot headed screws holding the transistor heat sinks.
- Unfasten the seven slot headed screws holding the P.C.B., the board may now be lifted out of the unit.

3.5.14. Removal of the Digital to Analog Converter printed circuit board

- Remove wrap round cover and rear panel (section 3.5.2.).
- Unplug all of the interface cables.
- Remove the four slot headed screws, the board may now be lifted out of the unit.

3.5.15. Removal of the microprocessor printed circuit board

- Remove wrap round cover and rear panel (section 3.5.2.).
- Remove connectors and leads from component side of board.
- The board can now be removed, taking care to clear the front panel switches.
- If it is found necessary to remove the microprocessor (Fig. 3.44) or the E-proms (Fig. 3.44.) great care must be taken to avoid bending the pins or breaking the encapsulation of the devices.

3.5.16. Removal of IC's fitted in sockets

When an integrated circuit is removed, because of the possibility of damaging either the pins or the printed circuit board the following system is recommended: cut a piece of thin card-board and slide it under the integrated circuit (Fig. 3.32.), use a screwdriver on alternate ends to obtain a straight lift.
(The card-board prevents the tracks underneath the integrated circuit from being damaged.)

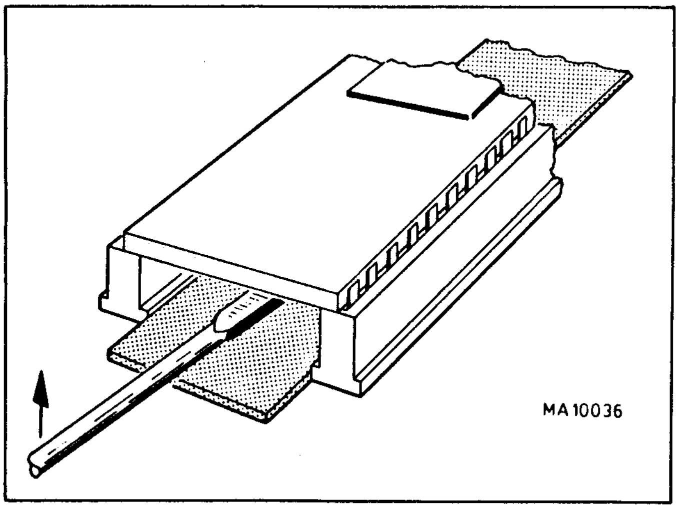


Fig. 3.32. Removing integrated circuit

3.5.17. Removal of I.C.'s soldered on p.c. board

- Cut by means of a pair of cutters the soldering pins from the body of the defective I.C.
- Carefully unsolder one after the other the soldering pins of the p.c. board.
- Remove all superfluous soldering material. Use a sucking iron or sucking copper litze-wire.
- Check that the pin of the replacement part are clear or pre-tinned on the soldering places.
- Locate the replacement I.C. exactly on its place, and solder the new I.C. on to the p.c. board.

NOTE: Bear in mind that the maximum permissible soldering time is 10 seconds during which the temperature of the I.C. must not exceed 250 deg C. The use of a solder with a low melting point is therefore recommended.

Take care, not to damage the plastic encapsulation of these parts during the soldering procedure (softening point of the plastic is 150 °C).

ATTENTION: When you are soldering inside the instrument it is essential to use a low-voltage soldering iron, the tip of which must be earthed to the mass of the instrument.

Suitable soldering irons are:
- ORYX micro-miniature soldering instrument, type 6A, voltage 6 V, in combination with PLATO pin-point tip type 0-569.
- ERSA miniature soldering iron, type minor 040 B, voltage 6 V.
- Low Voltage Mini Soldering Iron, Type 800/12 W - 6 V, power 12 W, voltage 6 V, order no. 4822 395 10004, in combination with 1 mm-pin-point tip, order no. 4822 395 10012.

3.6. EXTRA IN- AND OUTPUT CIRCUITS

The PM 3540 can be equipped with a Z-Mod. input, a time-base sweep output, a time-base gate output and an analyzer trigger output, mounted at the rear panel. These facilities can be composed of the following components. The in- and output BNC sockets are mounted in the holes above the c.r.t. socket; only 15-mm-holes must be drilled in the plastic rear cover (Fig. 3.33.) on the positions as indicated.

3.6.1. External Z-modulation input

Characteristics

- TTL Compatible
- Current drain at 0 V: –3 mA; at +5 V: +1 mA
- Brightness: light from +2 V to +7 V maximum
  dark from +0.8 V to –1.2 V minimum
- Rise time from light to dark and vice versa: 50 ns
- Delay time from input socket to screen: 82 ns

Used components

– Coax. cable (per metre)	5322 320 10003
– BNC connector	5322 267 10004
– Filler ring for BNC connector	5322 532 24319
– Nut for BNC connector	5322 506 14001
– Solder tag	5322 290 34022

3.6.2. Time-base sweep output

Characteristics

- Output voltage: minimum level –1,8 V
  maximum level +3,8 V ± 0,5 V
- Internal resistance: 1 kohm
- The output is protected against short-circuits

Required components

– Coax. cable (per metre)	5322 320 10003
– BNC connector	5322 267 10004
– Filler ring for BNC connector	5322 532 24319
– Nut for BNC connector	5322 506 14001
– Resistor 1 kohm	5322 116 54549
– Resistor 1.27 kohm	5322 116 50555
– Transistor BC548C	5322 130 44196
– Solder tag	5322 290 34022

3.6.3. Time-base gate output

Characteristics

- Output voltage: high level more than +2.7 V
  low level less than 0.5 V
- TTL output via 50 ohm resistor
- The output is protected against short-circuits

Required components

– Coax. cable (per metre)	5322 320 10003
– BNC connector	5322 267 10004
– Filler ring for BNC connector	5322 532 24319
– Nut for BNC connector	5322 506 14001
– Resistor 51.1 ohm	5322 116 54442
– Solder tag	5322 290 34022

3.6.4. Analyzer trigger output

- It is also possible to create a trigger output for a signal which is generated when triggerword is recognised.
- This signal can be taken from point 8 of gate D2034 and fed in a resistor of 100 Ω to a rearside mounted output socket.

Required components

– Coax. cable (per metre)	5322 320 10003
– BNC connector	5322 267 10004
– Filler ring for BNC connector	5322 532 24319
– Nut for BNC connector	5322 506 14001
– Resistor 100 ohm	5322 116 54469
– Solder tag	5322 290 34022

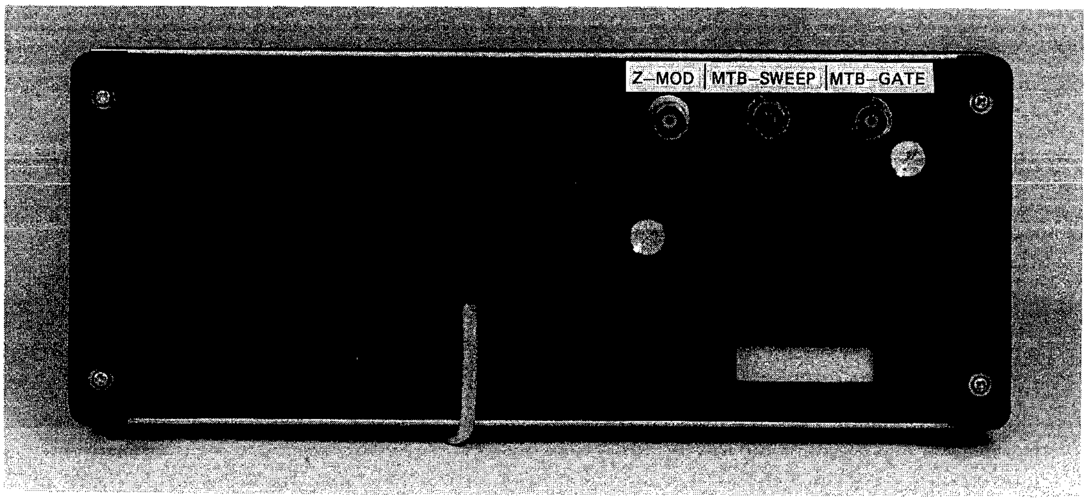


Fig. 3.33. Rear view of the instrument

3.7. INFORMATION CONCERNING ACCESSORIES

3.7.1. Logic Pod PM 8820 (analyzer probe)

The PM 8820 is a compact 8 bit Logic Pod for use with, for example the Logic-scope PM 3540.
It contains 8 identical high speed level detectors, with a common wide-range threshold, featuring high input impedances and TTL compatible outputs. Power should be obtained from the instrument it is used with.

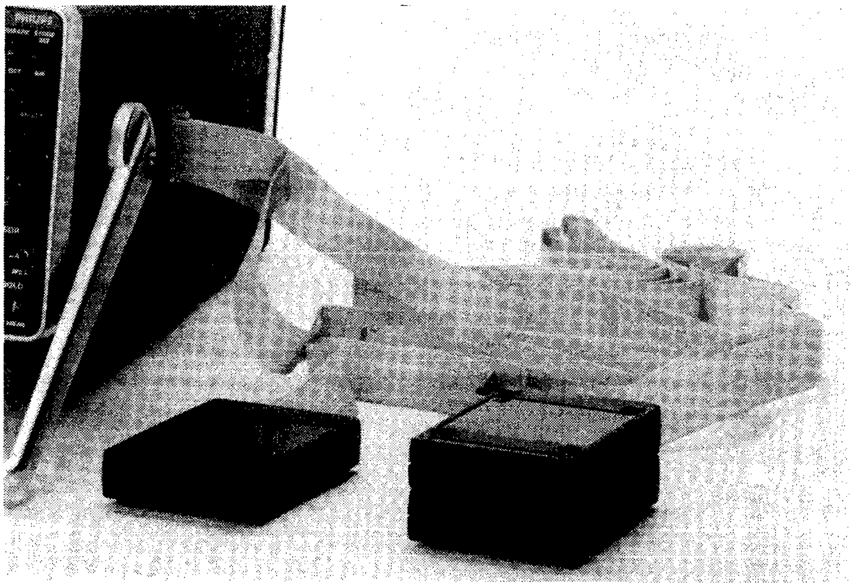


Fig. 3.34. Logic Pod PM 8820

3.7.2. Trimming Tool Kit (Type 800/NTX)

This useful kit contains 3 twin-coloured holders, 2 extension holders and 21 interchangeable trimming pins. The wide variety of pins allows almost every type of trimming function to be carried out in instruments to be calibrated (e.g. measuring instruments, radio and T.V. sets).

Ordering number: 4822 310 50015.
(A spare set containing the 8 most commonly used pins is available under the Ordering number: 4822 310 50016).

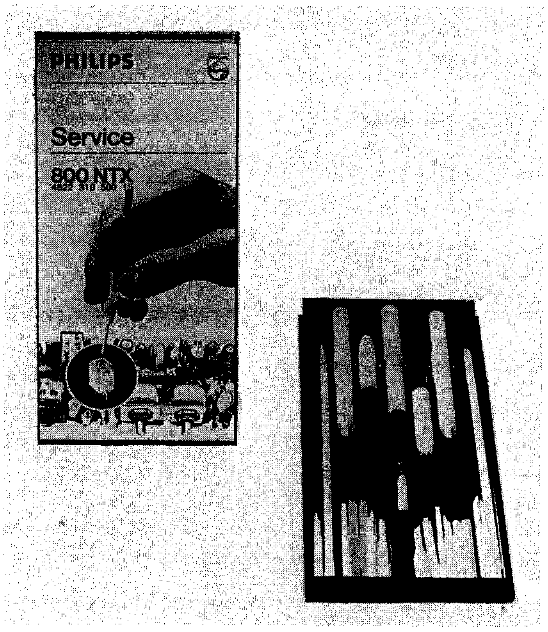


Fig. 3.35. Trimming tool kit

NOTES:

3.7.3. 1:10 Attenuator probe sets PM 8925(L) and PM 8927(L) oscilloscope probes

The PM 8925 and PM 8927 are 10x attenuator probes designed for oscilloscopes up to 35 MHz, having a BNC input jack and 15 to 40 pF input capacitance, paralleled by 1 MΩ. The L version is a similar probe with a cable length of 2.5 m.

The set consists of:

1 cable assembly	Fig. 3.36. item 1
1 spring-loaded test clip	Fig. 3.36. item 2
1 wire wrap adapter	Fig. 3.36. item 3
1 protective cap for probe tip	Fig. 3.36. item 4
1 dual in-line adapter	Fig. 3.36. item 5
2 probe tips	Fig. 3.36. item 6
1 earthing cord	Fig. 3.36. item 7
1 probe holder	Fig. 3.36. item 8
5 soldering terminals	Fig. 3.36. item 9
marking rings	Fig. 3.36. item 10
probe assembly	Fig. 3.36. item 11

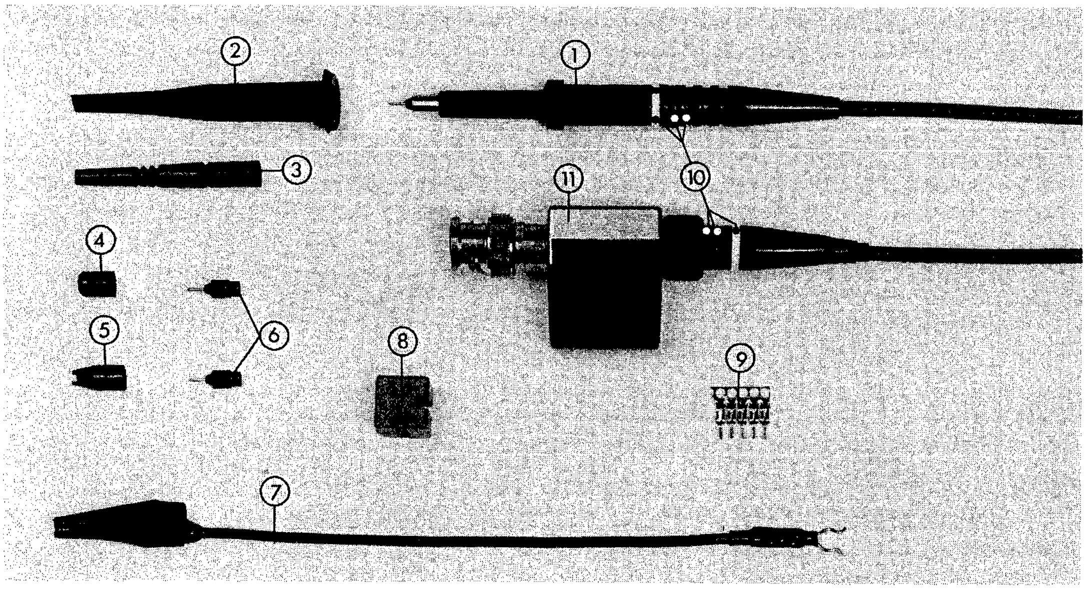


Fig. 3.36. Attenuator probe set PM 8925(L) or PM 8927(L)

3.7.3.1. Technical data

	PM 8925	PM 8925L	PM 8927	PM 8927L
Attenuation	10 x	10 x	10 x	10 x
Input resistance	10 MΩ	10 MΩ	10 MΩ	10 MΩ
Input capacity	11 pF	14 pF	11 pF	14 pF
Probe only rise time	3 ns	3.5 ns	1.7 ns	2 ns
Compensation range	15...40 pF	15...40 pF	14...21 pF	14...21 pF
Max. input voltage (DC + ACpk)	500 V	500 V	500 V	500 V
Cable length	1.5 m	2.5 m	1.5 m	2.5 m

3.7.3.2. Adjustment

The measuring probe has been adjusted and checked by the factory. However, to match the probe to your instrument, the following adjustment is necessary.
Connect the measuring pin to socket CAL of the instrument.
A trimmer can be adjusted through a hole in the compensation box to obtain optimum square-wave response.

See the following examples.

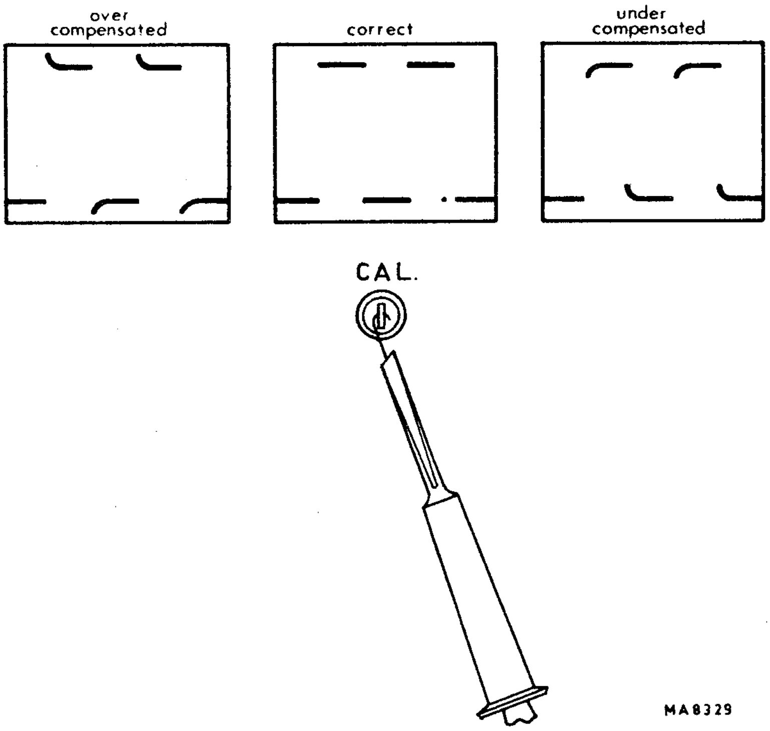


Fig. 3.37. Probe compensation

3.7.3.3. *Parts of attenuator probe sets PM 8925(L) and PM 8927(L)*

Item	*Qty.*	*Ordering code*	*Description*
1	1	5322 320 14063	Cable assembly
2	1	5322 264 24019	Spring-loaded test clip
3	1	5322 264 24018	Wrap pin adaptor
4	1	5322 462 44319	Protective cap
5	2	5322 462 44318	Dual in-line adapter
6	2	5322 268 14017	Probe tip
7	1	5322 321 20223	Earth cable
8	1	5322 256 94136	Probe holder
9	25	5322 255 44026	Soldering terminals
10	2	5322 532 64223	Marking ring red
10	2	5322 532 64224	Marking ring white
10	2	5322 532 64225	Marking ring blue

3.7.4. 1:1 Probe sets PM 8921 and PM 8921L (oscilloscope probe)

The PM 8921 is a passive probe without signal attenuation for use with oscilloscope, counters and voltmeters having a high input impedance and a BNC input socket.
The cable design is such that the reflection due to the instrument's capacitive load are absorbed.
The useful range of this probe is restricted to d.c. and l.f. application (up to 15 MHz).
The PM 8921L is a similar probe with a cable length of 2,5 m.

The set consists of:

1 probe assembly	Fig. 3.38. item 1
1 spring-loaded test clip	Fig. 3.38. item 2
1 wire wrap adapter	Fig. 3.38. item 3
1 protective cap for probe tip	Fig. 3.38. item 4
1 dual in-line adapter	Fig. 3.38. item 5
2 spare probe tips	Fig. 3.38. item 6
1 earthing lead	Fig. 3.38. item 7
1 probe holder	Fig. 3.38. item 8
5 soldering terminals	Fig. 3.38. item 9
marking rings	Fig. 3.38. item 10

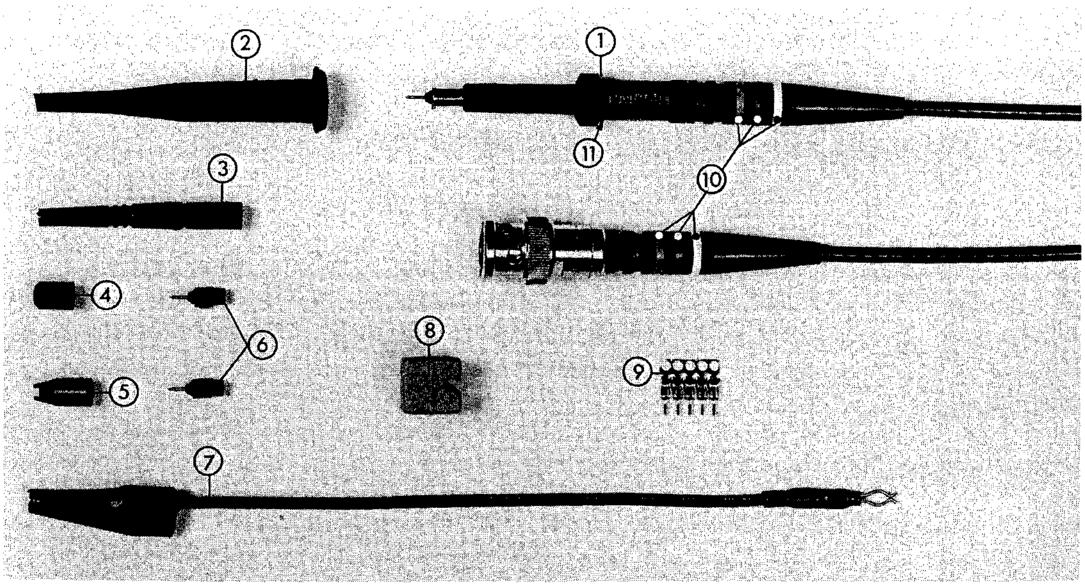


Fig. 3.38. Probe set PM 8921 (PM 8921L)

3.7.4.1. Technical data

	PM 8921	PM 8921L
Attenuation	1 x	1 x
Input resistance	1 MΩ	1 MΩ
Input capacity	42 pF	64 pF
Probe-only bandwidth	25 MHz	15 MHz
Probe-only rise time	17 ns	21 ns
Max. input voltage	500 V_{DC} + AC	500 V_{DC} + ACpk
Cable length	1.5 m	2.5 m

3.7.4.2. Parts of probe set PM 8921

Item	*Qty.*	*Ordering code*	*Description*
1	1	5322 264 24022	Probe shell
2	1	5322 264 24019	Spring-loaded test clip
3	1	5322 264 24018	Wire wrap adaptor
4	1	5322 462 44319	Protective cap
5	1	5322 462 44318	Dual in-line adapter
6	1	5322 268 14017	Probe tip
7	1	5322 321 20223	Earthing lead
8	1	5322 256 94136	Probe holder
9	25	5322 255 44026	Soldering terminals
10	2	5322 532 64223	Marking ring red
10	2	5322 532 64224	Marking ring white
10	2	5322 532 64225	Marking ring blue
11	1	5322 265 24033	Resistor assy

3.7.5. High-voltage probe set PM 8932

The PM 8932 is a 100x attenuator probe which can handle signals up to 5.6 V AC_{p-p}. The probe has beeen designed for use with oscilloscope having a bandwidth up to 150 MHz, a BNC input jack and an input impedance of 1 MΩ paralleled by 10 to 30 pF.

The set consists of:

1 cable assembly	Fig. 3.39. item 1
1 probe shell assy	Fig. 3.39. item 2
1 spring loaded test clip	Fig. 3.39. item 3
1 cover	Fig. 3.39. item 4
1 protective cap	Fig. 3.39. item 5
2 spare test pins	Fig. 3.39. item 6
1 earthing cable	Fig. 3.39. item 7
1 probe holder	Fig. 3.39. item 8
25 soldering terminals	Fig. 3.39. item 9
marking rings	Fig. 3.39. item 10

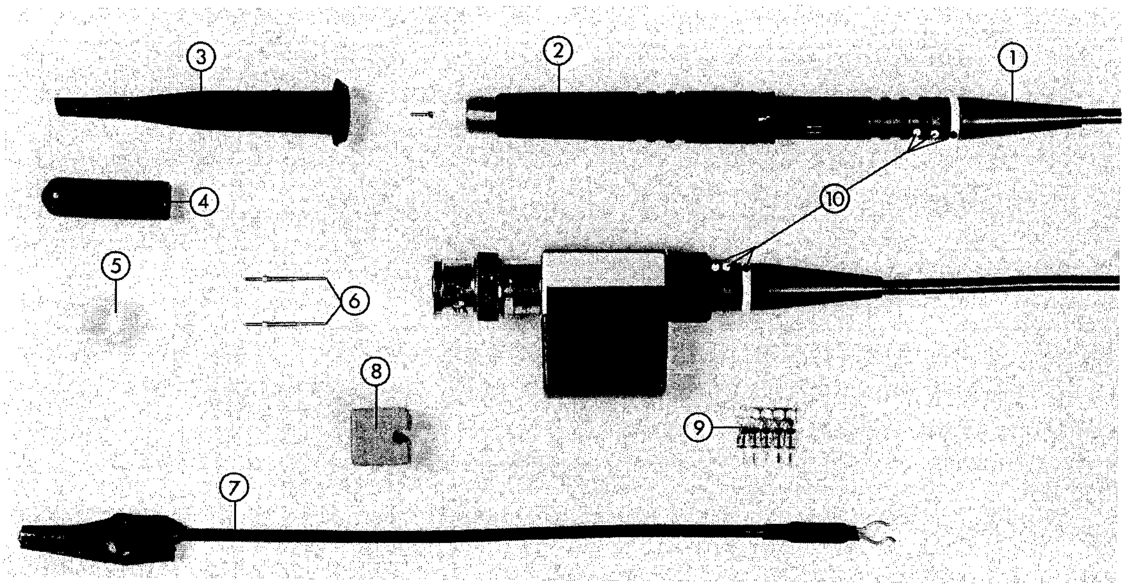


Fig. 3.39. Attenuator probe set PM 8932

3.7.5.1. *Technical data*

Attenuation	1:100 ± 2 %
Input resistance	20 MΩ ± 2 %
Input capacitance	2 pF ± 0,5 pF
Max. allowable voltage	DC or DC + AC_{p-p} continuous 4 kV
Sinewaves continuous	(for frequencies up to 1 MHz) 5,6 kV_{p-p}

3.7.5.2. *Adjustment*

The measuring probe has been adjusted and checked by the factory. However, to match the probe to your oscilloscope, the following manipulation is necessary. Connect the measuring pin to socket CAL of the instrument. A trimmer can be adjusted through a hole in the compensation box to obtain optimum square-wave response.

See the following examples:

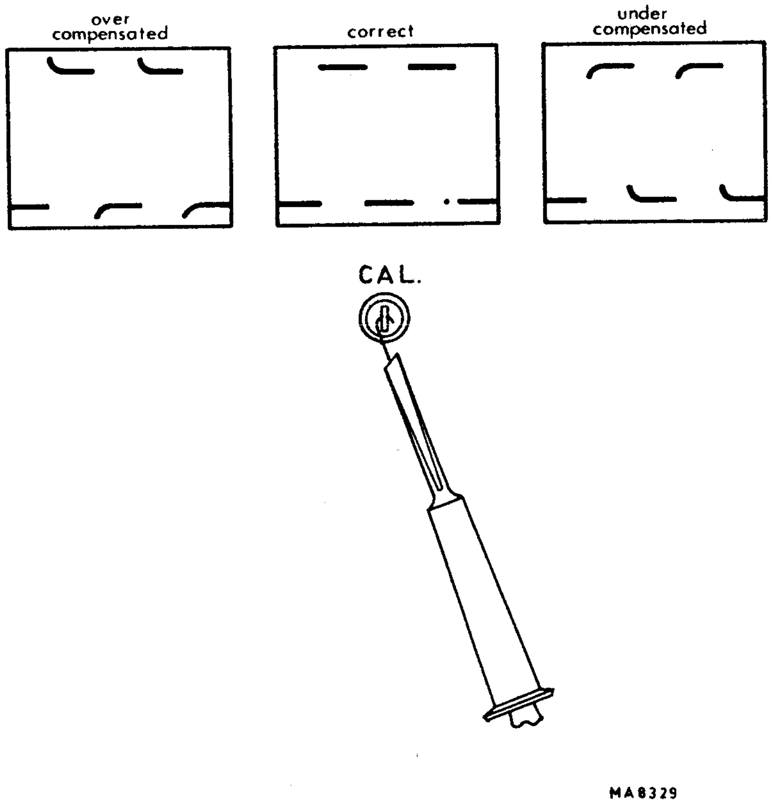
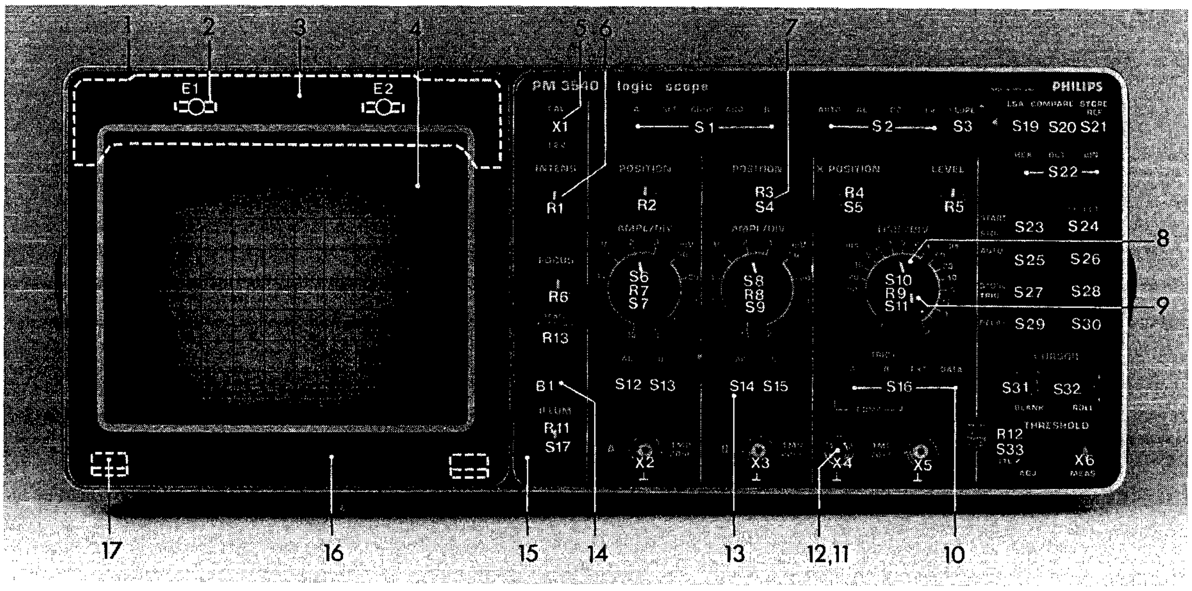


Fig. 3.40. Probe compensation

3.7.5.3. *Parts of probe set PM 8932*

Item	*Qty.*	*Ordering number*	*Description*
1	1	5322 320 14088	Cable assembly
2	1	5322 256 94143	Probe shell assy
3	1	5322 264 24023	Spring loaded test clip
4	1	5322 462 44074	Cover
5	1	5322 462 54075	Protective cap
6	2	5322 258 14119	Pin
7	1	5322 321 20223	Earth cable
8	1	5322 256 94136	Probe holder
9	25	5322 255 44026	Soldering terminals
10	2	5322 532 64223	Marking ring red
10	2	5322 532 64224	Marking ring white
10	2	5322 532 64225	Marking ring blue

3.8. PARTS LISTS AND DIAGRAMS (subject to alteration without notice)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16
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12,11
E1
E2
PM 3540
logic scope
PHILIPS
LSA
COMPARE
STORE
REF
X1
S1
S2
S3
S19
S20
S21
INTENS
POSITION
X POSITION
LEVEL
R1
R2
R3
S4
R4
S5
R5
S22
S23
S24
START
AUTO
S25
S26
S27
S28
S29
S30
FOCUS
R6
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R7
S7
S8
R8
S9
S10
R9
S11
R13
B1
S12
S13
S14
S15
TRIG
DATA
S16
CURSOR
S31
S32
BLANK
ROLL
THRESHOLD
R12
S33
ADJ
MEAS
ILLUM
R11
S17
X2
X3
X4
X5
X6

Fig. 3.41. Front view showing item numbers

3.8.1. Mechanical Parts

	Item	*Qty.*	*Ordering number*	*Designation*
Fig. 3.41.				
	1	1	5322 447 94401	Cast aluminium front frame
	2	2	5322 255 24015	Lamp holder
	3	2	5322 381 14151	Reflector
	4	1	5322 480 34074	Contrast filter blue
	5	4	5322 325 84013	Grommet (for X1 and X6)
	6	8	5322 414 34134	Knob (dia 10)
		7	5322 414 74015	Knob cover (grey)
		8	5322 492 64337	Retaining spring
	7	2	5322 414 34091	Knob (dia 10)
	8	3	5322 414 34079	Knob (dia 18.7)
	9	3	5322 414 74029	Knob cover (blue)
	10	27	5322 414 14011	Knob square (grey)
	11	1	5322 505 14178	Knurled nut
	12	1	5322 506 14005	Hexagonal nut
	13	1	5322 414 25613	Knob square (grey-green)
	14	5	5322 255 44088	LED Holder
	15	1	5322 455 84086	Text plate
	16	2	5322 450 74009	Bezel
	17	2	5322 492 64629	Bezel clamp spring

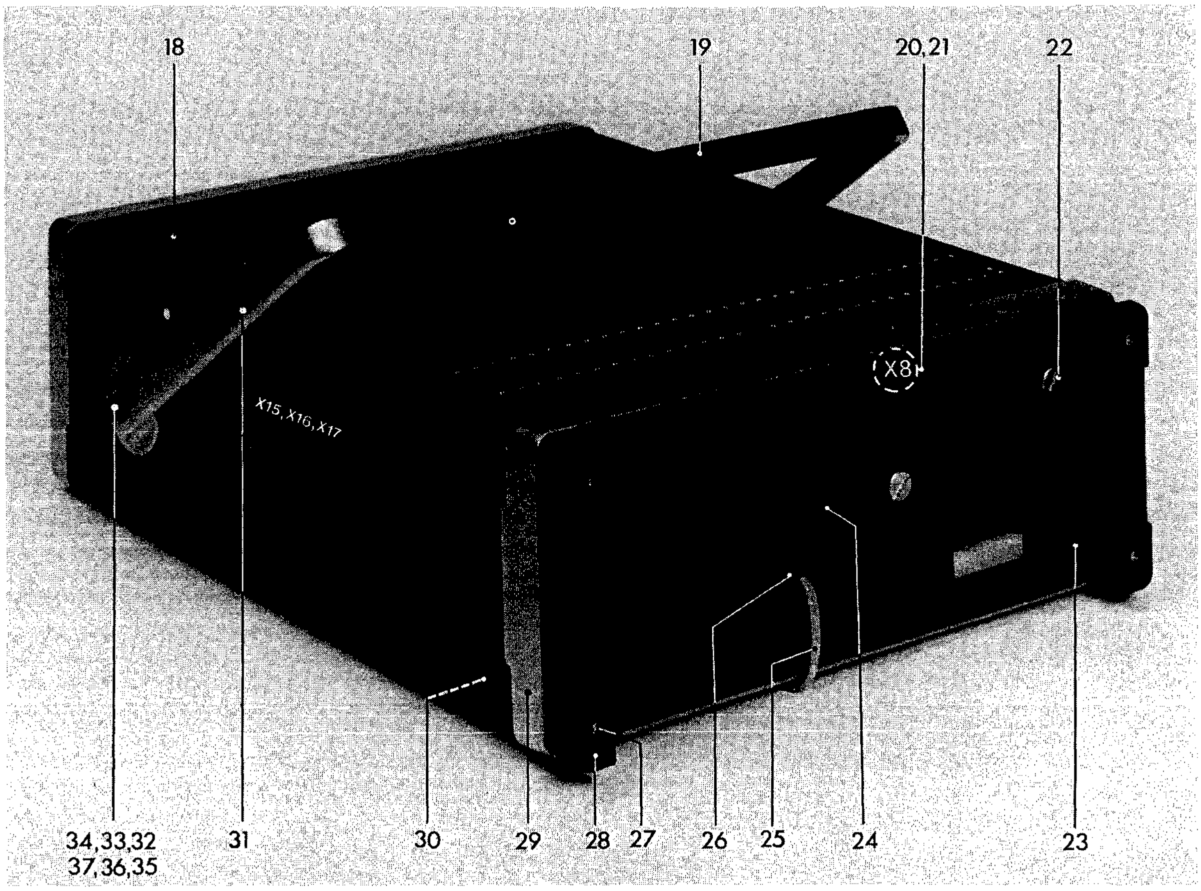

Fig. 3.42. Side view showing item numbers

Fig. 3.42.

18	1	5322 455 84087	Cabinet without handle
19	1	5322 498 54077	Grip
20	1	5322 506 14001	Nut (for X8)
21	1	5322 532 24319	Padding ring (for X8)
22	2	5322 500 14228	Coin slot screw
23	1	5322 447 94599	Rear panel
24	1	4822 272 10079	Line voltage adaptor
25	1	4822 321 10084	Line cable (Eur.)
	1	4822 321 10092	Line cable (U.S.A.)
26	1	5322 325 64083	Line cable cleat
27	4	5322 462 44374	Hole plug
28	2	5322 462 44298	Foot
29	1	5322 447 94402	Cast aluminium rear frame
30	4	5322 462 44297	Foot
31	2	5322 498 54072	Carrying handle
32	2	5322 414 64053	Knob
33	2	4822 502 30054	Screw
34	2	4822 532 10582	Washer
35	2	5322 528 34128	Ratched
36	2	5322 530 84075	Spring
37	2	5322 520 14267	Bearing bush

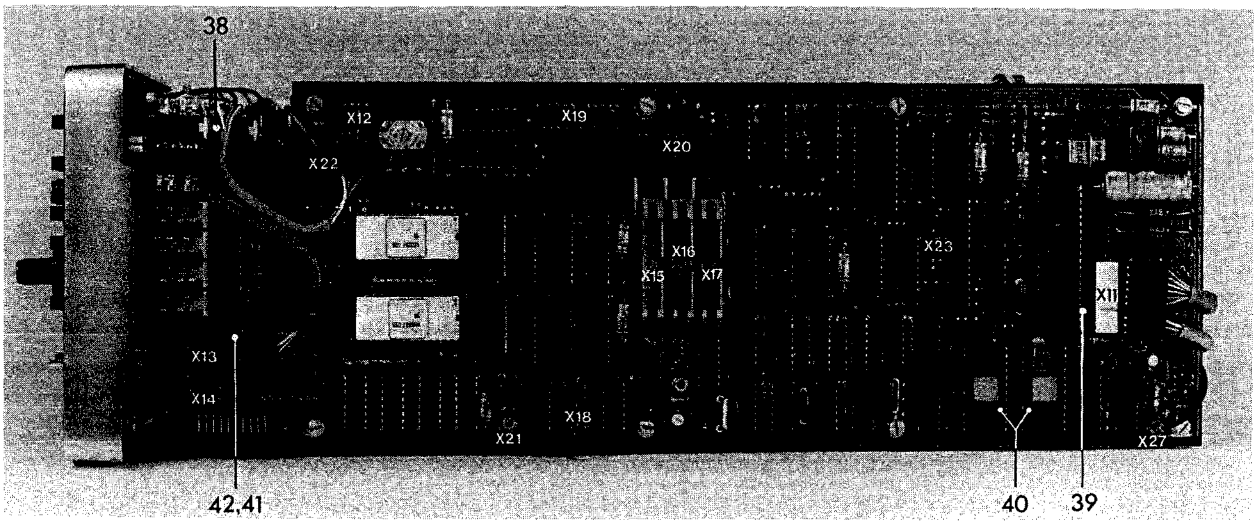

Fig. 3.43. Inside view showing item numbers

Fig. 3.43.

38	1	5322 216 54242	Logic switch (complete with wiring)
39	1	5322 209 84872	I.C. socket
40	2	5322 255 44109	I.C. socket
41		5322 268 14013	Pin contact for P.W. connector
42		5322 401 14191	Polarity key

Not shown

5322 447 94403	Front cover
5322 532 74014	Ring composite of V1
5322 535 74594	Extension shaft for S23, S25, S27, S29
5322 276 14102	Self-releasing push-button segment
5322 276 14117	Mutual-releasing push-button segment
5322 325 64051	Grommet 7 x 2 (rubber)
5322 705 34066	Insulating plate for potm. FOCUS
4822 255 40115	Insulating material for trans. V207

3.8.2. ELECTRICAL PARTS PM3540

ITEM	ORDERING NUMBER	FARAD	TOL (%)	VOLTS	REMARKS
CAPACITORS					
C 0	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1	5322 122 14018				CERAMIC TUBULAR
C 2	5322 125 54003				TRIMMER
C 11	4822 122 31045	4,7PF	0,25PF	100	CERAMIC PLATE
C 12	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 13	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 14	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 17	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 21	4822 122 31045	4,7PF	0,25PF	100	CERAMIC PLATE
C 22	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 27	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 31	4822 122 31045	4,7PF	0,25PF	100	CERAMIC PLATE
C 32	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 33	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 34	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 37	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 41	4822 122 31045	4,7PF	0,25PF	100	CERAMIC PLATE
C 42	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 47	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 51	4822 122 31045	4,7PF	0,25PF	100	CERAMIC PLATE
C 52	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 53	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 54	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 57	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 61	4822 122 31045	4,7PF	0,25PF	100	CERAMIC PLATE
C 62	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 67	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 71	4822 122 31045	4,7PF	0,25PF	100	CERAMIC PLATE
C 72	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 73	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 74	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 77	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 81	4822 122 31045	4,7PF	0,25PF	100	CERAMIC PLATE
C 82	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 87	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 91	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 92	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 93	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 94	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 95	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 96	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 97	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 98	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 99	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 101	5322 121 44189	330NF		250	POLYESTER FOIL
C 200	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 201	4822 122 30099	3,3NF	10	100	CERAMIC PLATE
C 202	4822 121 40443	680NF	10	100	POLYESTER FOIL
C 203	4822 124 70226	4700UF	–10+50	40	ELECTROLYTIC
C 204	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 207	4822 121 40443	680NF	10	100	POLYESTER FOIL
C 208	4822 124 20699	47UF	–10+50	25	ELECTROLYTIC
C 209	4822 124 20697	10UF	–10+50	25	ELECTROLYTIC
C 211	4822 124 20671	68UF	–10+50	6,3	ELECTROLYTIC
C 212	5322 122 54004	470PF	20	4000	CERAMIC DISK
C 213	5322 122 54004	470PF	20	4000	CERAMIC DISK
C 214	5322 122 54004	470PF	20	4000	CERAMIC DISK
C 216	5322 122 54004	470PF	20	4000	CERAMIC DISK
C 217	5322 122 54004	470PF	20	4000	CERAMIC DISK
C 218	4822 121 40196	22NF	10	1600	POLYESTER FOIL
C 219	4822 121 40196	22NF	10	1600	POLYESTER FOIL
C 221	4822 124 20316	4UF	-10+50	250	ELECTROLYTIC
C 222	4822 124 20715	100UF	-10+50	40	ELECTROLYTIC
C 223	4822 124 20688	33UF	-10+50	16	ELECTROLYTIC
C 224	4822 124 20693	220UF	-10+50	16	ELECTROLYTIC
C 226	4822 124 20671	68UF	-10+50	6,3	ELECTROLYTIC
C 227	4822 124 20673	470UF	-10+50	6,3	ELECTROLYTIC
C 228	4822 124 20688	33UF	-10+50	16	ELECTROLYTIC

ITEM	ORDERING NUMBER	FARAD	TOL (%)	VOLTS	REMARKS
C 229	4822 124 20693	220UF	-10+50	16	ELECTROLYTIC
C 231	4822 124 20316	4UF	-10+50	250	ELECTROLYTIC
C 301	4822 121 40012	100NF	10	400	POLYESTER FOIL
C 305	4822 122 31072	47PF	2	500	CERAMIC PLATE
C 307	5322 125 50051	18PF		300	TRIMMER
C 308	4822 122 31072	47PF	2	500	CERAMIC PLATE
C 309	4822 122 31197	15PF	2	500	CERAMIC PLATE
C 310	4822 122 31197	15PF	2	500	CERAMIC PLATE
C 311	4822 122 31196	12PF	2	500	CERAMIC PLATE
C 312	4822 122 31217	3,9PF	0,25PF	500	CERAMIC PLATE
C 313	5322 125 54027	5,5PF		400	TRIMMER
C 314	5322 125 54027	5,5PF		400	TRIMMER
C 315	4822 122 31184	1,5PF	0,25PF	500	CERAMIC PLATE
C 316	5322 125 54026	3PF		400	TRIMMER
C 317	5322 125 54026	3PF		400	TRIMMER
C 318	5322 125 54027	5,5PF		400	TRIMMER
C 319	5322 125 54026	3PF		400	TRIMMER
C 320	4822 122 31188	3,3PF	0,25PF	500	CERAMIC PLATE
C 321	4822 122 30045	27PF	2	100	CERAMIC PLATE
C 322	4822 122 31247	120PF	2	100	CERAMIC PLATE
C 324	4822 122 31247	120PF	2	100	CERAMIC PLATE
C 351	4822 122 31199	22PF	2	500	CERAMIC PLATE
C 352	4822 122 30045	27PF	2	100	CERAMIC PLATE
C 353	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 354	4822 122 31036	2,2PF	0,25PF	100	CERAMIC PLATE
C 357	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 358	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 401	4822 121 40012	100NF	10	400	POLYESTER FOIL
C 405	4822 122 31072	47PF	2	500	CERAMIC PLATE
C 407	5322 125 50051	18PF		300	TRIMMER
C 408	4822 122 31072	47PF	2	500	CERAMIC PLATE
C 409	4822 122 31197	15PF	2	500	CERAMIC PLATE
C 410	4822 122 31197	15PF	2	500	CERAMIC PLATE
C 411	4822 122 31196	12PF	2	500	CERAMIC PLATE
C 412	4822 122 31217	3,9PF	0,25PF	500	CERAMIC PLATE
C 413	5322 125 54027	5,5PF		400	TRIMMER
C 414	5322 125 54027	5,5PF		400	TRIMMER
C 415	4822 122 31184	1,5PF	0,25PF	500	CERAMIC PLATE
C 416	5322 125 54026	3PF		400	TRIMMER
C 417	5322 125 54026	3PF		400	TRIMMER
C 418	5322 125 54027	5,5PF		400	TRIMMER
C 419	5322 125 54026	3PF		400	TRIMMER
C 420	4822 122 31188	3,3PF	0,25PF	500	CERAMIC PLATE
C 421	4822 122 30045	27PF	2	100	CERAMIC PLATE
C 422	4822 122 31247	120PF	2	100	CERAMIC PLATE
C 424	4822 122 31247	120PF	2	100	CERAMIC PLATE
C 501	4822 122 31072	47PF	2	100	CERAMIC PLATE
C 502	4822 125 50045	22PF		100	TRIMMER
C 503	4822 122 30113	180PF	2	100	CERAMIC PLATE
C 504	4822 122 31047	5,6PF	0,25PF	100	CERAMIC PLATE
C 507	5322 125 50048	3,5PF		300	TRIMMER
C 509	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 511	4822 122 31054	10PF	2	100	CERAMIC PLATE
C 513	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 517	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 518	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 519	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 521	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 522	4822 122 31085	150PF	2	100	CERAMIC PLATE
C 523	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 524	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 527	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 528	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 529	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 530	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 531	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 532	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 601	4822 122 31072	47PF	2	100	CERAMIC PLATE
C 602	4822 125 50045	22PF		100	TRIMMER
C 603	4822 122 30113	180PF	2	100	CERAMIC PLATE

ITEM	ORDERING NUMBER	FARAD	TOL (%)	VOLTS	REMARKS
C 604	4822 122 31047	5,6PF	0,25PF	100	CERAMIC PLATE
C 607	5322 125 50048	3,5PF		30	TRIMMER
C 609	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 611	4822 122 31054	10PF	2	100	CERAMIC PLATE
C 613	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 616	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 617	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 618	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 619	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 621	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 622	4822 122 31085	150PF	2	100	CERAMIC PLATE
C 623	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 627	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 629	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 630	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 631	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 632	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 701	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 702	4822 122 31168	270PF	10	100	CERAMIC PLATE
C 703	4822 122 31174	2,7NF	10	100	CERAMIC PLATE
C 704	4822 122 31174	2,7NF	10	100	CERAMIC PLATE
C 705	4822 122 31125	4,7NF	-20+80	40	CERAMIC PLATE
C 706	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 707	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 709	4822 122 31081	100PF	2	500	CERAMIC PLATE
C 801	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 802	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 803	4822 121 41134	10NF	10	250	POLYESTER FOIL
C 804	4822 122 30113	180PF	2	100	CERAMIC PLATE
C 805	4822 122 30104	1PF	0,25PF	100	CERAMIC PLATE
C 806	4822 122 31175	1NF	10	100	CERAMIC PLATE
C 807	4822 122 31074	56PF	2	100	CERAMIC PLATE
C 808	4822 122 31076	68PF	2	100	CERAMIC PLATE
C 809	4822 125 50045	22PF		100	TRIMMER
C 810	4822 122 30104	1PF	0,25PF	100	CERAMIC PLATE
C 811	4822 125 50045	22PF		100	TRIMMER
C 812	4822 122 31067	33PF	2	100	CERAMIC PLATE
C 813	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 814	4822 122 31054	10PF	2	100	CERAMIC PLATE
C 815	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 816	4822 122 31054	10PF	2	100	CERAMIC PLATE
C 818	5322 125 50048	3,5PF		300	TRIMMER
C 821	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1001	4822 121 40438	470NF	10	100	POLYESTER FOIL
C 1002	4822 121 40438	470NF	10	100	POLYESTER FOIL
C 1003	4822 121 40427	220NF	10	100	POLYESTER FOIL
C 1004	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1006	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 1007	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1008	5322 122 34039	0,56PF	0,25PF	100	CERAMIC PLATE
C 1011	4822 122 30128	4,7NF	10	100	CERAMIC PLATE
C 1012	4822 122 30128	4,7NF	10	100	CERAMIC PLATE
C 1013	4822 122 30098	3,9NF	10	100	CERAMIC PLATE
C 1016	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 1017	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1018	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 1019	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 1201	4822 122 31085	150PF	2	100	CERAMIC PLATE
C 1202	4822 121 40423	150NF	10	100	POLYESTER FOIL
C 1203	4822 122 31168	270PF	10	100	CERAMIC PLATE
C 1204	5322 121 54054	2,4NF	1	63	POLYSTYRENE FOIL
C 1205	4822 122 31243	82PF	2	100	CERAMIC PLATE
C 1206	4822 122 31414	10NF	-20+50	100	CERAMIC PLATE
C 1207	5322 121 44246	2,2UF	5	100	POLYESTER FOIL
C 1208	4822 124 20726	4,7UF	-10+50	63	ELECTROLYTIC
C 1209	4822 122 31175	1NF	10	100	CERAMIC PLATE
C 1210	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1211	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1212	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1213	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC

ITEM	ORDERING NUMBER	FARAD	TOL (%)	VOLTS	REMARKS
C 1214	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 1216	4822 124 20687	15UF	-10+50	16	ELECTROLYTIC
C 1401	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1402	4822 122 31347	100PF	2	100	CERAMIC PLATE
C 1404	4822 121 40427	220NF	10	100	POLYESTER FOIL
C 1406	5322 122 34039	0,56PF	0,25PF	100	CERAMIC PLATE
C 1407	5322 122 34039	0,56PF	0,25PF	100	CERAMIC PLATE
C 1408	5322 122 34039	0,56PF	0,25PF	100	CERAMIC PLATE
C 1409	5322 125 50048	3,5PF		300	TRIMMER
C 1411	4822 122 30103	22NF	–20+80	40	CERAMIC PLATE
C 1412	4822 122 30103	22NF	–20+80	40	CERAMIC PLATE
C 1413	4822 121 40407	220NF	10	250	POLYESTER FOIL
C 1414	4822 122 30103	22NF	–20+80	40	CERAMIC PLATE
C 1416	4822 121 40407	22NF	10	250	POLYESTER FOIL
C 1417	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 1418	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 1419	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 1421	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 1501	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1502	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1503	4822 122 30103	22NF	-20+80	40	CERAMIC PLATE
C 1504	4822 122 30104	1PF	0,25PF	100	CERAMIC PLATE
C 1506	4822 122 30043	10NF	–20+80	40	CERAMIC PLATE
C 1507	4822 121 41134	10NF	–20+80	250	POLYESTER FOIL
C 1508	4822 122 30099	3,3NF	–20+80	100	CERAMIC PLATE
C 1509	4822 121 40354	1,5NF	0,25PF	1600	POLYESTER FOIL
C 1511	4822 122 30103	22NF	–20+80	40	CERAMIC PLATE
C 1512	4822 121 40354	1,5NF	10	1600	POLYESTER FOIL
C 1513	4822 121 40354	1,5NF	10	1600	POLYESTER FOIL
C 1601	4822 121 40434	1,5NF	10	1600	POLYESTER FOIL
C 1602	4822 122 31072	47PF	2	100	CERAMIC PLATE
C 2004	4822 122 31081	100PF	2	100	CERAMIC PLATE
C 2005	4822 122 31074	56PF	2	100	CERAMIC PLATE
C 2006	4822 122 31061	18PF	2	100	CERAMIC PLATE
C 2008	4822 122 31072	47PF	2	100	CERAMIC PLATE
C 2009	4822 122 31177	470PF	10	100	CERAMIC PLATE
C 2011	4822 122 31081	100PF	2	100	CERAMIC PLATE
C 2012	4822 121 41161	100PF	10	250	POLYESTER FOIL
C 2051	4822 122 31063	22PF	2	100	CERAMIC PLATE
C 2052	4822 122 31063	22PF	2	100	CERAMIC PLATE
C 2053	4822 124 20709	15UF	-10+50	40	ELECTROLYTIC
C 2054	4822 124 20688	33UF	-10+50	16	ELECTROLYTIC
C 2056	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2057	4822 124 20688	33UF	–10+50	16	ELECTROLYTIC
C 2058	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2059	4822 124 20688	33UF	–10+50	16	ELECTROLYTIC
C 2061	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2062	4822 124 20768	100UF	–10+50	10	ELECTROLYTIC
C 2063	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2064	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2066	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2067	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2068	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2069	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2071	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2072	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2073	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2074	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2076	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2077	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 2078	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 2079	4822 124 20688	33UF	-10+50	16	ELECTROLYTIC
C 2081	4822 124 20688	33UF	-10+50	16	ELECTROLYTIC
C 2082	4822 124 20688	33UF	-10+50	16	ELECTROLYTIC
C 2083	4822 124 20688	33UF	-10+50	16	ELECTROLYTIC
C 2084	4822 124 20688	33UF	-10+50	16	ELECTROLYTIC
C 2086	4822 124 20688	33UF	-10+50	16	ELECTROLYTIC
C 2087	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 2088	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 2102	4822 122 31175	1NF	10	100	CERAMIC PLATE
C 2103	4822 122 30043	10NF	-20+80	40	CERAMIC PLATE
C 2104	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2106	4822 124 20688	33UF	–10+50	16	ELECTROLYTIC
C 2107	4822 122 30043	10NF	–20+80	40	CERAMIC PLATE
C 2108	4822 122 31081	100PF	2	100	CERAMIC PLATE
C 2152	4822 121 41161	100NF	10	250	POLYESTER FOIL
C 2153	4822 124 20688	33UF	–10+50	16	ELECTROLYTIC

ITEM	ORDERING NUMBER	OHM	TOL (%)	TYPE	REMARKS
RESISTORS					
R 1	5322 101 24117	10K	20	0.1W	CARBON POTM LIN
R 2	5322 101 24118	1K	20	0.1W	CARBON POTM LIN
R 3+S4	5322 101 64018	1K	20	0.1W	CARBON POTM LIN + SWITCH
R 4+S5	5322 102 44004	2x47K	20		CARBON TANDEM POTM + SWITCH
R 5	4822 101 20457	100K	20	0.1W	CARBON POTM LIN
R 6	5322 101 24098	2,2M	20	0.1W	CARBON POTM LIN
R 7+S7	5322 101 44024	1K	20	0.1W	CARBON POTM LIN + SWITCH
R 8+S9	5322 101 44024	1K	20	0.1W	CARBON POTM LIN + SWITCH
R 9+S11	5322 101 44023	10K	20		CARBON POTM LIN + SWITCH
R 11	5322 101 44025	22K	20	0.1W	CARBON POTM LIN + SWITCH
R 12	5322 101 54013	10K	20	0.1W	CARBON POTM LOG + SWITCH
R 13	5322 101 20408	100K	20	0,1W	CARBON POTM LIN
R 16	5322 116 50904	30,1	1	MR25	METAL FILM
R 17	5322 116 54714	154K	1	MR25	METAL FILM
R 21	5322 116 64025	4M	1	SPEC	METAL OXIDE
R 22	5322 116 55284	681K	1	MR25	METAL FILM
R 26	5322 116 50904	30,1	1	MR25	METAL FILM
R 27	5322 116 54714	154K	1	MR25	METAL FILM
R 31	5322 116 64025	4M	1	SPEC	METAL OXIDE
R 32	5322 116 55284	681K	1	MR25	METAL FILM
R 36	5322 116 50904	30,1	1	MR25	METAL FILM
R 37	5322 116 54714	154K	1	MR25	METAL FILM
R 41	5322 116 64025	4M	1	SPEC	METAL OXIDE
R 42	5322 116 55284	681K	1	MR25	METAL FILM
R 46	5322 116 50904	30,1	1	MR25	METAL FILM
R 47	5322 116 54714	154K	1	MR25	METAL FILM
R 51	5322 116 64025	4M	1	SPEC	METAL OXIDE
R 52	5322 116 55284	681K	1	MR25	METAL FILM
R 56	5322 116 50904	30,1	1	MR25	METAL FILM
R 57	5322 116 54714	154K	1	MR25	METAL FILM
R 61	5322 116 64025	4M	1	SPEC	METAL OXIDE
R 62	5322 116 55284	681K	1	MR25	METAL FILM
R 66	5322 116 50904	30,1	1	MR25	METAL FILM
R 67	5322 116 54714	154K	1	MR25	METAL FILM
R 71	5322 116 64025	4M	1	SPEC	METAL OXIDE
R 72	5322 116 55284	681K	1	MR25	METAL FILM
R 76	5322 116 50904	30,1	1	MR25	METAL FILM
R 77	5322 116 54714	154K	1	MR25	METAL FILM
R 81	5322 116 64025	4M	1	SPEC	METAL OXIDE
R 82	5322 116 55284	681K	1	MR25	METAL FILM
R 86	5322 116 50904	30,1	1	MR25	METAL FILM
R 87	5322 116 54714	154K	1	MR25	METAL FILM
R 91	5322 116 50675	2,26K	1	MR25	METAL FILM
R 92	5322 116 50636	2,74K	1	MR25	METAL FILM
R 93	5322 116 50675	2,26K	1	MR25	METAL FILM
R 94	5322 116 50675	2,26K	1	MR25	METAL FILM
R 96	4822 116 51169	562K	1	MR25	METAL FILM
R 97	5322 116 50567	95,3K	1	MR25	METAL FILM
R 200	4822 116 51253	10K	1	MR25	METAL FILM
R 201	5322 116 54646	23,7K	1	MR25	METAL FILM
R 202	5322 116 54557	1,21K	1	MR25	METAL FILM
R 203	4822 166 51235	1K	1	MR25	METAL FILM
R 204	5322 101 14051	220	20	0.5W	TRIMMING POTM
R 206	5322 116 55279	2,87K	1	MR25	METAL FILM
R 207	5322 116 50636	2,74K	1	MR25	METAL FILM
R 208	5322 116 50904	30,1	1	MR25	METAL FILM
R 209	5322 116 50904	30,1	1	MR25	METAL FILM
R 210	5322 116 55275	1M	1	MR30	METAL FILM
R 211	5322 111 50345	8,2M	5	1W	CARBON
R 212	5322 116 51253	10K	1	MR25	METAL FILM
R 227	5322 116 50679	237	1	MR25	METAL FILM
R 302	5322 116 55275	1M	1	MR30	METAL FILM
R 303	5322 116 54469	100	1	MR25	METAL FILM
R 304	5322 116 54459	75	1	MR25	METAL FILM
R 306	5322 116 54459	75	1	MR25	METAL FILM
R 307	5322 116 55319	191K	1	MR30	METAL FILM
R 308	5322 116 54263	681K	1	MR30	METAL FILM
R 309	5322 116 55379	845K	1	MR30	METAL FILM

ITEM	ORDERING NUMBER	OHM	TOL (%)	TYPE	REMARKS
R 311	5322 116 55139	549K	1	MR30	METAL FILM
R 312	5322 116 55387	205K	1	MR25	METAL FILM
R 313	5322 116 55321	732K	1	MR30	METAL FILM
R 314	5322 116 55078	806K	1	MR30	METAL FILM
R 316	4822 110 63212	8,2M	10	CR25	CARBON
R 317	5322 116 55275	1M	1	MR30	METAL FILM
R 318	5322 116 50859	90,9K	0,25	MR24C	METAL FILM
R 319	5322 116 50979	8,25K	0,25	MR24C	METAL FILM
R 354	5322 116 55078	806K	1	MR30	METAL FILM
R 356	5322 101 14069	22K	20	0.5W	TRIMMING POTM
R 357	5322 116 55419	20,5K	1	MR25	METAL FILM
R 358	5322 101 14069	22K	20	0.5W	TRIMMING POTM
R 359	5322 116 55419	20,5K	1	MR25	METAL FILM
R 361	5322 101 14069	22K	20	0.5W	TRIMMING POTM
R 362	5322 116 55419	20,5K	1	MR25	METAL FILM
R 363	5322 116 54558	8,25K	1	MR25	METAL FILM
R 364	5322 116 55448	4,02K	1	MR25	METAL FILM
R 365	5322 116 54192	5,11	1	MR25	METAL FILM
R 366	5322 116 50581	2,49K	1	MR25	METAL FILM
R 367	5322 116 55359	1,62K	1	MR25	METAL FILM
R 368	5322 116 54192	5,11	1	MR25	METAL FILM
R 369	5322 116 55359	1,62K	1	MR25	METAL FILM
R 370	5322 116 50452	10	1	MR25	METAL FILM
R 371	5322 116 50452	10	1	MR25	METAL FILM
R 374	5322 116 50452	10	1	MR25	METAL FILM
R 376	5322 116 54692	86,6K	1	MR25	METAL FILM
R 377	5322 116 54442	51,1	1	MR25	METAL FILM
R 402	5322 116 55275	1M	1	MR30	METAL FILM
R 403	5322 116 54469	100	1	MR25	METAL FILM
R 404	5322 116 54459	75	1	MR25	METAL FILM
R 406	5322 116 54459	75	1	MR25	METAL FILM
R 407	5322 116 55319	191K	1	MR30	METAL FILM
R 408	5322 116 54263	681K	1	MR30	METAL FILM
R 409	5322 116 55379	845K	1	MR30	METAL FILM
R 411	5322 116 55139	549K	1	MR30	METAL FILM
R 412	5322 116 55387	205K	1	MR25	METAL FILM
R 413	5322 116 55321	732K	1	MR30	METAL FILM
R 414	5322 116 55078	806K	1	MR30	METAL FILM
R 416	4822 110 63212	8,2M	10	CR25	CARBON
R 417	5322 116 55275	1M	1	MR30	METAL FILM
R 418	5322 116 50859	90,9K	0,25	MR24C	METAL FILM
R 419	5322 116 50979	8,25K	0,25	MR24C	METAL FILM
R 500	5322 116 54442	51,1	1	MR25	METAL FILM
R 501	5322 116 54442	51,1	1	MR25	METAL FILM
R 502	5322 116 55078	806K	1	MR30	METAL FILM
R 503	5322 116 50443	12,7K	1	MR25	METAL FILM
R 504	5322 101 14047	470	20	0,5W	TRIMMING POTM
R 506	5322 116 50443	12,7K	1	MR25	METAL FILM
R 507	5322 116 55426	6,19K	1	MR25	METAL FILM
R 508	5322 116 54603	6,49K	1	MR25	METAL FILM
R 509	4822 116 51232	619	1	MR25	METAL FILM
R 511	4822 116 51282	511	0,5	MR25	METAL FILM
R 512	4822 116 51282	511	0,5	MR25	METAL FILM
R 513	5322 116 54472	105	1	MR25	METAL FILM
R 514	5322 101 14069	22K	20	0.5W	TRIMMING POTM
R 516	5322 116 50672	51,1K	1	MR25	METAL FILM
R 517	5322 116 50583	5,9K	1	MR25	METAL FILM
R 518	5322 116 54545	909	1	MR25	METAL FILM
R 519	5322 116 50417	162	1	MR25	METAL FILM
R 521	5322 100 10112	1K	20	0,5W	TRIMMING POTM
R 522	5322 116 50818	44,2	1	MR25	METAL FILM
R 523	5322 116 50818	44,2	1	MR25	METAL FILM
R 524	5322 116 54469	100	1	MR25	METAL FILM
R 526	5322 116 54469	100	1	MR25	METAL FILM
R 527	4822 116 51281	5,62K	0,5	MR25	METAL FILM
R 528	5322 116 55278	909	0,5	MR25	METAL FILM
R 529	5322 116 54442	51,1	1	MR25	METAL FILM
R 531	5322 116 54442	51,1	1	MR25	METAL FILM
R 532	5322 116 55278	909	0,5	MR25	METAL FILM
R 533	4822 116 51281	5,62K	0,5	MR25	METAL FILM

ITEM	ORDERING NUMBER	OHM	TOL (%)	TYPE	REMARKS
R 534	5322 116 54541	825	1	MR25	METAL FILM
R 535	5322 116 54541	825	1	MR25	METAL FILM
R 536	5322 116 50904	30,1	1	MR25	METAL FILM
R 537	5322 116 54543	866	1	MR25	METAL FILM
R 538	5322 116 34054	1,5K	5	0.5W	NTC
R 539	5322 116 50904	30,1	1	MR25	METAL FILM
R 540	5322 116 54519	402	1	MR25	METAL FILM
R 541	5322 116 54515	348	1	MR25	METAL FILM
R 542	5322 116 54499	249	1	MR25	METAL FILM
R 543	5322 101 14011	100	20	0,5W	TRIMMING POTM
R 546	5322 116 54547	953	1	MR25	METAL FILM
R 547	5322 101 14009	220	20	0,5W	TRIMMING POTM
R 548	5322 116 54547	953	1	MR25	METAL FILM
R 549	5322 116 54469	100	1	MR25	METAL FILM
R 550	5322 116 50452	10	1	MR25	METAL FILM
R 551	5322 116 54469	100	1	MR25	METAL FILM
R 552	5322 116 54426	121	1	MR25	METAL FILM
R 553	5322 116 54426	121	1	MR25	METAL FILM
R 554	5322 116 55278	909	1	MR25	METAL FILM
R 558	5322 116 54637	17,8K	1	MR25	METAL FILM
R 559	5322 116 54595	5,11K	1	MR25	METAL FILM
R 568	5322 116 54637	17,8K	1	MR25	METAL FILM
R 569	5322 116 50583	5,9K	1	MR25	METAL FILM
R 571	5322 116 54492	178	1	MR25	METAL FILM
R 572	5322 116 54492	178	1	MR25	METAL FILM
R 573	5322 116 50675	2,26K	1	MR25	METAL FILM
R 577	5322 116 54469	100	1	MR25	METAL FILM
R 581	5322 116 50568	4,99	1	MR25	METAL FILM
R 582	5322 116 50568	4,99	1	MR25	METAL FILM
R 583	5322 116 50568	4,99	1	MR25	METAL FILM
R 584	5322 116 50568	4,99	1	MR25	METAL FILM
R 586	5322 116 50568	4,99	1	MR25	METAL FILM
R 587	5322 116 50568	4,99	1	MR25	METAL FILM
R 600	5322 116 54442	51,1	1	MR25	METAL FILM
R 601	5322 116 54442	51,1	1	MR25	METAL FILM
R 602	5322 116 55078	806K	1	MR30	METAL FILM
R 603	5322 116 50443	12,7K	1	MR25	METAL FILM
R 604	5322 101 14047	470	20	0,5W	TRIMMING POTM
R 606	5322 116 50443	12,7K	1	MR25	METAL FILM
R 607	5322 116 55426	6,19K	1	MR25	METAL FILM
R 608	5322 116 54603	6,49K	1	MR25	METAL FILM
R 609	5322 116 51232	619	1	MR25	METAL FILM
R 611	4822 116 51282	511	0,5	MR25	METAL FILM
R 612	4822 116 51282	511	0,5	MR25	METAL FILM
R 613	5322 116 54472	105	1	MR25	METAL FILM
R 614	5322 101 14069	22K	20	0.5W	TRIMMING POTM
R 616	5322 116 50672	51,1K	1	MR25	METAL FILM
R 617	5322 116 50583	5,9K	1	MR25	METAL FILM
R 618	5322 116 55278	909	1	MR25	METAL FILM
R 619	5322 116 50417	162	1	MR25	METAL FILM
R 621	5322 100 10112	1K	20	0,5W	TRIMMING POTM
R 622	5322 116 50818	44,2	1	MR25	METAL FILM
R 623	5322 116 50818	44,2	1	MR25	METAL FILM
R 624	5322 116 54469	100	1	MR25	METAL FILM
R 626	5322 116 54469	100	1	MR25	METAL FILM
R 627	4822 116 51281	5,62K	0,5	MR25	METAL FILM
R 628	5322 116 55278	909	0,5	MR25	METAL FILM
R 629	5322 116 54442	51,1	1	MR25	METAL FILM
R 631	5322 116 54442	51,1	1	MR25	METAL FILM
R 632	5322 116 55278	909	0,5	MR25	METAL FILM
R 633	4822 116 51281	5,62K	0,5	MR25	METAL FILM
R 634	5322 116 54541	825	1	MR25	METAL FILM
R 635	5322 116 54541	825	1	MR25	METAL FILM
R 636	5322 116 50904	30,1	1	MR25	METAL FILM
R 637	5322 116 54543	866	1	MR25	METAL FILM
R 638	5322 116 34054	1,5K	5	0.5W	NTC
R 639	5322 116 50904	30,1	1	MR25	METAL FILM
R 640	5322 116 54519	402	1	MR25	METAL FILM
R 641	5322 116 55418	158	0,5	MR25	METAL FILM
R 646	4822 116 51235	1K	1	MR25	METAL FILM

ITEM	ORDERING NUMBER	OHM	TOL (%)	TYPE	REMARKS
R 647	5322 101 14011	100	20	0,5W	TRIMMING POTM
R 648	4822 116 51235	1K	1	MR25	METAL FILM
R 649	5322 116 54469	100	1	MR25	METAL FILM
R 650	5322 116 50452	10	1	MR25	METAL FILM
R 651	5322 116 54469	100	1	MR25	METAL FILM
R 652	5322 116 54426	121	1	MR25	METAL FILM
R 653	5322 116 54426	121	1	MR25	METAL FILM
R 654	5322 116 55278	909	1	MR25	METAL FILM
R 658	5322 116 54637	17,8K	1	MR25	METAL FILM
R 659	5322 116 54595	5,11K	1	MR25	METAL FILM
R 661	5322 116 54657	31,6K	1	MR25	METAL FILM
R 662	5322 116 54637	17,8K	1	MR25	METAL FILM
R 663	5322 116 54629	14K	1	MR25	METAL FILM
R 664	5322 116 54558	8,25K	1	MR25	METAL FILM
R 668	5322 116 54637	17,8K	1	MR25	METAL FILM
R 669	5322 116 50583	5,9K	1	MR25	METAL FILM
R 671	5322 116 54492	178	1	MR25	METAL FILM
R 672	5322 116 54492	178	1	MR25	METAL FILM
R 673	5322 116 50675	2,26K	1	MR25	METAL FILM
R 674	5322 101 14048	47K	20	0,5W	TRIMMING POTM
R 676	4822 116 51259	33,2K	1	MR25	METAL FILM
R 677	5322 116 54469	100	1	MR25	METAL FILM
R 682	5322 116 50568	4,99	1	MR25	METAL FILM
R 683	5322 116 50568	4,99	1	MR25	METAL FILM
R 684	5322 116 50568	4,99	1	MR25	METAL FILM
R 701	5322 116 54469	100	1	MR25	METAL FILM
R 702	5322 116 50555	1,27K	1	MR25	METAL FILM
R 703	4822 116 51234	750	1	MR25	METAL FILM
R 704	5322 116 54519	402	1	MR25	METAL FILM
R 705	5322 116 50568	4,99	1	MR25	METAL FILM
R 706	5322 116 50555	1,27K	1	MR25	METAL FILM
R 707	5322 116 55419	20,5K	1	MR25	METAL FILM
R 708	4822 116 51252	6,81K	1	MR25	METAL FILM
R 709	5322 116 50581	2,49K	1	MR25	METAL FILM
R 710	5322 116 50568	4,99	1	MR25	METAL FILM
R 711	5322 116 50581	2,49K	1	MR25	METAL FILM
R 712	5322 116 55448	4,02K	1	MR25	METAL FILM
R 713	5322 116 55448	4,02K	1	MR25	METAL FILM
R 714	5322 116 55448	4,02K	1	MR25	METAL FILM
R 716	5322 116 55448	4,02K	1	MR25	METAL FILM
R 717	5322 116 54852	100	1	MR30	METAL FILM
R 801	5322 116 55448	4,02K	1	MR25	METAL FILM
R 802	5322 116 54558	8,25K	1	MR25	METAL FILM
R 803	5322 116 54469	100	1	MR25	METAL FILM
R 804	5322 116 54469	100	1	MR25	METAL FILM
R 806	5322 116 54426	121	1	MR25	METAL FILM
R 807	5322 116 54426	121	1	MR25	METAL FILM
R 808	5322 116 50671	2,61K	1	MR25	METAL FILM
R 809	5322 116 55422	1,33K	1	MR25	METAL FILM
R 811	5322 116 50458	7,87K	1	MR25	METAL FILM
R 812	5322 101 14008	2,2K	20	0.5W	TRIMMING POTM
R 813	5322 100 10114	4,7K	20	0.5W	TRIMMING POTM
R 814	5322 100 10112	1K	20	0,5W	TRIMMING POTM
R 816	5322 116 50904	30,1	1	MR25	METAL FILM
R 817	4822 100 10075	100	20	0.05W	TRIMMING POTM
R 818	5322 116 50904	30,1	1	MR25	METAL FILM
R 819	5322 116 54068	28,7	1	MR25	METAL FILM
R 821	5322 116 54068	28,7	1	MR25	METAL FILM
R 823	5322 116 54489	169	1	MR25	METAL FILM
R 824	5322 116 50458	7,87K	1	MR25	METAL FILM
R 825	5322 116 50568	4,99	1	MR25	METAL FILM
R 826	5322 116 50675	2,26K	1	MR25	METAL FILM
R 827	5322 116 50729	4,22K	1	MR25	METAL FILM
R 828	5322 116 54469	100	1	MR25	METAL FILM
R 829	5322 116 54469	100	1	MR25	METAL FILM
R 831	5322 116 54464	86,6	1	MR25	METAL FILM
R 832	5322 116 54464	86,6	1	MR25	METAL FILM
R 833	5322 116 55278	909	1	MR25	METAL FILM
R 837	5322 116 55278	909	1	MR25	METAL FILM
R 838	5322 116 54557	1,21K	1	MR25	METAL FILM

ITEM	ORDERING NUMBER	OHM	TOL (%)	TYPE	REMARKS
R 839	5322 116 54557	1,21K	1	MR25	METAL FILM
R 843	4822 116 51233	681	1	MR25	METAL FILM
R 847	5322 116 54466	90,9	1	MR25	METAL FILM
R 848	5322 101 14011	100	20	0,5W	TRIMMING POTM
R 849	5322 116 54466	90,9	1	MR25	METAL FILM
R 851	5322 116 54466	90,9	1	MR25	METAL FILM
R 852	5322 116 50818	44,2	1	MR25	METAL FILM
R 853	5322 116 50818	44,2	1	MR25	METAL FILM
R 854	5322 116 54466	90,9	1	MR25	METAL FILM
R 856	5322 116 54484	140	1	MR25	METAL FILM
R 857	5322 116 55367	3,48K	1	MR25	METAL FILM
R 858	5322 116 51246	3,01K	1	MR25	METAL FILM
R 859	5322 116 50515	1,78K	1	MR25	METAL FILM
R 861	5322 116 50515	1,78K	1	MR25	METAL FILM
R 862	5322 116 50515	1,78K	1	MR25	METAL FILM
R 863	5322 116 50515	1,78K	1	MR25	METAL FILM
R 1001	5322 116 50672	51,1K	1	MR25	METAL FILM
R 1002	5322 116 50672	51,1K	1	MR25	METAL FILM
R 1003	5322 116 50672	51,1K	1	MR25	METAL FILM
R 1004	5322 116 50672	51,1K	1	MR25	METAL FILM
R 1006	5322 116 54587	3,65K	1	MR25	METAL FILM
R 1007	5322 116 54558	8,25K	1	MR25	METAL FILM
R 1008	5322 116 54743	301K	1	MR25	METAL FILM
R 1009	5322 116 54123	511K	1	MR30	METAL FILM
R 1011	5322 116 55448	4,02K	1	MR25	METAL FILM
R 1012	5322 116 51268	100K	1	MR25	METAL FILM
R 1013	5322 116 50443	12,7K	1	MR25	METAL FILM
R 1014	5322 101 14047	470	20	0,5W	TRIMMING POTM
R 1016	5322 116 50443	12,7K	1	MR25	METAL FILM
R 1017	5322 116 55279	2,87K	1	MR25	METAL FILM
R 1018	4822 116 51231	562	1	MR25	METAL FILM
R 1019	4822 116 51231	562	1	MR25	METAL FILM
R 1021	5322 116 54587	3,65K	1	MR25	METAL FILM
R 1022	5322 116 50586	1,54K	1	MR25	METAL FILM
R 1023	5322 116 50586	1,54K	1	MR25	METAL FILM
R 1024	5322 116 50904	30,1	1	MR25	METAL FILM
R 1026	5322 116 50904	30,1	1	MR25	METAL FILM
R 1027	4822 116 51232	619	1	MR25	METAL FILM
R 1028	4822 116 51232	619	1	MR25	METAL FILM
R 1029	5322 116 50731	10,5K	1	MR25	METAL FILM
R 1031	5322 116 55448	4,02K	1	MR25	METAL FILM
R 1032	5322 116 50572	12,1K	1	MR25	METAL FILM
R 1033	4822 116 51235	1K	1	MR25	METAL FILM
R 1034	5322 116 55361	16,2K	1	MR25	METAL FILM
R 1036	5322 116 54587	3,65K	1	MR25	METAL FILM
R 1037	5322 116 54558	8,25K	1	MR25	METAL FILM
R 1038	5322 116 50671	2,61K	1	MR25	METAL FILM
R 1039	5322 116 55275	1M	1	MR30	METAL FILM
R 1041	5322 101 14069	22K	20	0.5W	TRIMMING POTM
R 1042	5322 116 55419	20,5K	1	MR25	METAL FILM
R 1043	5322 116 54562	1,4K	1	MR25	METAL FILM
R 1044	5322 116 50728	1,87K	1	MR25	METAL FILM
R 1046	4822 116 51253	10K	1	MR25	METAL FILM
R 1047	4822 116 51246	3,01K	1	MR25	METAL FILM
R 1048	5322 116 55275	1M	1	MR30	METAL FILM
R 1049	5322 116 50484	4,64K	1	MR25	METAL FILM
R 1051	5322 116 55364	196K	1	MR25	METAL FILM
R 1052	5322 116 50583	5,9K	1	MR25	METAL FILM
R 1053	5322 116 50568	4,99	1	MR25	METAL FILM
R 1054	5322 116 50568	4,99	1	MR25	METAL FILM
R 1056	5322 116 50568	4,99	1	MR25	METAL FILM
R 1201	4822 116 51268	100K	1	MR25	METAL FILM
R 1202	5322 116 50442	48,7K	1	MR25	METAL FILM
R 1203	5322 116 55367	3,48K	1	MR25	METAL FILM
R 1204	5322 116 55426	6,19K	1	MR25	METAL FILM
R 1207	5322 116 50452	10	1	MR25	METAL FILM
R 1208	4822 110 63201	3,3M	10	CR25	CARBON
R 1209	4822 116 51253	10K	1	MR25	METAL FILM
R 1211	5322 116 50581	2,49K	1	MR25	METAL FILM
R 1212	4822 116 51253	10K	1	MR25	METAL FILM

ITEM	ORDERING NUMBER	OHM	TOL (%)	TYPE	REMARKS
R 1213	5322 116 51233	681	1	MR25	METAL FILM
R 1214	5322 116 54595	5,11K	1	MR25	METAL FILM
R 1216	5322 116 54552	1,05K	1	MR25	METAL FILM
R 1217	5322 116 50458	7,87K	1	MR25	METAL FILM
R 1218	5322 116 55421	32,4	0,5	MR25	METAL FILM
R 1219	5322 116 50904	30,1	1	MR25	METAL FILM
R 1220	5322 116 50863	9,09	1	MR25	METAL FILM
R 1221	5322 116 54562	1,4K	1	MR25	METAL FILM
R 1222	5322 116 54617	9,53K	1	MR25	METAL FILM
R 1223	5322 116 55459	15,4K	1	MR25	METAL FILM
R 1224	5322 116 50904	30,1	1	MR25	METAL FILM
R 1226	5322 116 50586	1,54K	1	MR25	METAL FILM
R 1227	5322 116 54608	7,5K	1	MR25	METAL FILM
R 1228	5322 116 50458	7,87K	1	MR25	METAL FILM
R 1229	5322 116 55462	37,4K	1	MR25	METAL FILM
R 1230	5322 116 54651	26,1K	1	MR25	METAL FILM
R 1231	4822 116 51259	33,2K	1	MR25	METAL FILM
R 1232	4822 100 10051	22K	20	0.05W	TRIMMING POTM
R 1233	5322 116 54515	348	1	MR25	METAL FILM
R 1234	5322 116 50675	2,26K	1	MR25	METAL FILM
R 1236	5322 116 50451	21,5K	1	MR25	METAL FILM
R 1237	5322 116 50568	4,99	1	MR25	METAL FILM
R 1238	5322 116 50568	4,99	1	MR25	METAL FILM
R 1239	5322 116 50568	4,99	1	MR25	METAL FILM
R 1276	5322 116 55424	412K	0,5	MR25	METAL FILM
R 1277	5322 116 55387	205K	0,5	MR25	METAL FILM
R 1278	5322 116 55423	41,2K	0,5	MR25	METAL FILM
R 1279	5322 116 55428	8,06K	0,5	MR25	METAL FILM
R 1281	4822 116 51243	2K	0,5	MR25	METAL FILM
R 1282	5322 116 55422	365	0,5	MR25	METAL FILM
R 1283	5322 116 55424	412K	0,5	MR25	METAL FILM
R 1284	5322 116 55374	82,5K	0,5	MR25	METAL FILM
R 1286	5322 116 55419	20,5K	0,5	MR25	METAL FILM
R 1287	5322 116 54283	4,02K	0,1	MR24E	METAL FILM
R 1288	5322 116 55427	768	0,5	MR25	METAL FILM
R 1289	5322 116 55426	6,19K	0,5	MR25	METAL FILM
R 1290	5322 116 55382	953K	0,5	MR30	METAL FILM
R 1291	5322 116 54736	261K	0,5	MR25	METAL FILM
R 1401	5322 116 50579	3,16K	1	MR25	METAL FILM
R 1402	5322 116 54442	51,1	1	MR25	METAL FILM
R 1403	5322 116 55448	4,02K	1	MR25	METAL FILM
R 1404	5322 116 50579	3,16K	1	MR25	METAL FILM
R 1406	5322 116 54595	5,11K	1	MR25	METAL FILM
R 1407	4822 116 51233	681	1	MR25	METAL FILM
R 1408	5322 116 54558	8,25K	1	MR25	METAL FILM
R 1409	4822 116 51246	3,01K	1	MR25	METAL FILM
R 1411	4822 116 51284	9,09K	1	MR25	METAL FILM
R 1412	5322 116 54576	2,37K	1	MR25	METAL FILM
R 1414	4822 116 51246	3,01K	1	MR25	METAL FILM
R 1416	4822 116 51247	3,32K	1	MR25	METAL FILM
R 1417	5322 100 10112	1K	20	0,5W	TRIMMING POTM
R 1418	5322 116 54506	287	1	MR25	METAL FILM
R 1419	5322 101 14011	100	20	0,5W	TRIMMING POTM
R 1421	5322 116 54613	8,66K	1	MR25	METAL FILM
R 1422	5322 116 55361	16,2K	1	MR25	METAL FILM
R 1423	5322 116 55419	20,5K	1	MR25	METAL FILM
R 1424	5322 116 50726	36,5K	1	MR25	METAL FILM
R 1425	5322 116 54469	100	1	MR25	METAL FILM
R 1426	5322 116 50572	12,1K	1	MR25	METAL FILM
R 1427	5322 116 54714	154K	1	MR25	METAL FILM
R 1428	4822 116 51259	33,2K	1	MR25	METAL FILM
R 1429	4822 116 51259	33,2K	1	MR25	METAL FILM
R 1431	4822 116 51235	1K	1	MR25	METAL FILM
R 1432	4822 116 51259	33,2K	1	MR25	METAL FILM
R 1433	4822 116 51259	33,2K	1	MR25	METAL FILM
R 1434	5322 116 54714	154K	1	MR25	METAL FILM
R 1436	4822 116 51236	1,1K	1	MR25	METAL FILM
R 1437	5322 116 50904	30,1	1	MR25	METAL FILM
R 1438	4822 116 51246	3,01K	1	MR25	METAL FILM
R 1439	5322 116 50904	30,1	1	MR25	METAL FILM

ITEM	ORDERING NUMBER	OHM	TOL (%)	TYPE	REMARKS
R 1440	5322 116 54595	5,11K	1	MR25	METAL FILM
R 1441	4822 116 51236	1,1K	1	MR25	METAL FILM
R 1442	5322 116 55276	13,3K	1	MR25	METAL FILM
R 1443	5322 116 55426	6,19K	1	MR25	METAL FILM
R 1444	5322 116 54762	365K	1	MR30	METAL FILM
R 1445	5322 116 54595	5,11K	1	MR25	METAL FILM
R 1446	5322 116 54762	365K	1	MR30	METAL FILM
R 1447	5322 116 54469	100	1	MR25	METAL FILM
R 1448	5322 116 54469	100	1	MR25	METAL FILM
R 1450	5322 116 50514	64,9K	1	MR25	METAL FILM
R 1501	4822 116 51252	6,81K	1	MR25	METAL FILM
R 1502	5322 116 55318	511	1	MR25	METAL FILM
R 1503	5322 116 55367	3,48K	1	MR25	METAL FILM
R 1506	5322 116 54616	162K	1	MR25	METAL FILM
R 1507	5322 116 55367	3,48K	1	MR25	METAL FILM
R 1508	4822 116 51268	100K	1	MR25	METAL FILM
R 1509	5322 116 54623	11K	1	MR25	METAL FILM
R 1511	5322 116 50672	51,1K	1	MR25	METAL FILM
R 1512	5322 116 55426	6,19K	1	MR25	METAL FILM
R 1513	5322 116 54651	26,1K	1	MR25	METAL FILM
R 1514	5322 116 55426	6,19K	1	MR25	METAL FILM
R 1516	5322 116 50481	22,6K	1	MR25	METAL FILM
R 1517	5322 116 50664	2,05K	1	MR25	METAL FILM
R 1518	5322 116 55318	511	1	MR25	METAL FILM
R 1519	5322 116 50536	464	1	MR25	METAL FILM
R 1521	5322 116 54729	226K	1	MR25	METAL FILM
R 1522	5322 116 34049	680	5	0.5W	NTC
R 1523	5322 116 55448	4,02K	1	MR25	METAL FILM
R 1524	5322 116 54469	100	1	MR25	METAL FILM
R 1525	5322 116 54835	511	1	MR30	METAL FILM
R 1526	4822 116 51175	64,9K	1	MR30	METAL FILM
R 1527	5322 116 54637	17,8K	1	MR25	METAL FILM
R 1528	4822 116 51259	33,2K	1	MR25	METAL FILM
R 1529	5322 116 55445	4,87K	1	MR25	METAL FILM
R 1531	5322 116 55358	11,5K	1	MR25	METAL FILM
R 1532	5322 116 55275	1M	1	MR30	METAL FILM
R 1533	5322 116 54469	100	1	MR25	METAL FILM
R 1534	5322 100 10113	10K	20	0,5W	TRIMMING POTM
R 1535	5322 116 54207	1K	1	MR30	METAL FILM
R 1536	5322 116 50484	4,64K	1	MR25	METAL FILM
R 1537	5322 116 55275	1M	1	MR30	METAL FILM
R 1538	4822 110 42189	1,2M	5	VR37	CARBON
R 1539	4822 110 42196	2,2M	5	VR37	CARBON
R 1541	4822 110 42207	5,6M	5	VR37	CARBON
R 1542	5322 116 50533	78,7K	1	MR25	METAL FILM
R 1543	4822 100 10072	100K	20	0.05W	TRIMMING POTM
R 1544	5322 116 54704	121K	1	MR25	METAL FILM
R 1546	5322 116 55361	16,2K	1	MR25	METAL FILM
R 1547	5322 116 54651	26,1K	1	MR25	METAL FILM
R 1548	5322 116 55364	196K	1	MR25	METAL FILM
R 1549	4822 100 10103	1M	20	0.05W	TRIMMING POTM
R 1551	5322 116 54761	383K	1	MR30	METAL FILM
R 1552	5322 116 50568	4,99	1	MR25	METAL FILM
R 1553	5322 116 50568	4,99	1	MR25	METAL FILM
R 1554	5322 116 50568	4,99	1	MR25	METAL FILM
R 1601	5322 116 55366	301	1	MR25	METAL FILM
R 1602	5322 116 50572	12,1K	1	MR25	METAL FILM
R 1603	5322 116 50664	2,05K	1	MR25	METAL FILM
R 1604	4822 116 51253	10K	1	MR25	METAL FILM
R 1606	4822 116 51233	681	1	MR25	METAL FILM
R 1607	5322 116 14069	22K	20	0.5W	TRIMMING POTM
R 1608	5322 116 55369	38,3K	1	MR25	METAL FILM
R 1609	5322 116 54547	953	1	MR25	METAL FILM
R 1611	4822 116 51253	10K	1	MR25	METAL FILM
R 1612	4822 116 51233	681	1	MR25	METAL FILM
R 1613	5322 116 55426	6,19K	1	MR25	METAL FILM
R 1614	5322 116 55367	3,48K	1	MR25	METAL FILM
R 1616	5322 116 50664	2,05K	1	MR25	METAL FILM
R 1617	5322 116 55366	301	1	MR25	METAL FILM
R 1618	5322 116 54651	26,1K	1	MR25	METAL FILM

ITEM	ORDERING NUMBER	OHM	TOL (%)	TYPE	REMARKS
R 1619	5322 116 50572	12,1K	1	MR25	METAL FILM
R 2001	5322 116 54562	1,4K	1	MR25	METAL FILM
R 2002	5322 116 50586	1,54K	1	MR25	METAL FILM
R 2003	5322 116 54442	51,1	1	MR25	METAL FILM
R 2004	5322 116 55279	2,87K	1	MR25	METAL FILM
R 2006	5322 116 55279	2,87K	1	MR25	METAL FILM
R 2007	5322 116 55258	511K	1	MR25	METAL FILM
R 2008	5322 116 50567	95,3K	1	MR25	METAL FILM
R 2009	5322 116 54716	162K	1	MR25	METAL FILM
R 2011	5322 116 54571	1,96K	1	MR25	METAL FILM
R 2012	5322 116 54571	1,96K	1	MR25	METAL FILM
R 2013	5322 116 50572	12,1K	1	MR25	METAL FILM
R 2014	5322 116 55358	11,5K	1	MR25	METAL FILM
R 2015	5322 116 54694	90,9K	1	MR25	METAL FILM
R 2016	4822 116 51235	1K	1	MR25	METAL FILM
R 2017	4822 116 51235	1K	1	MR25	METAL FILM
R 2018	4822 116 51253	10K	1	MR25	METAL FILM
R 2019	4822 116 51235	1K	1	MR25	METAL FILM
R 2021	4822 116 51235	1K	1	MR25	METAL FILM
R 2022	4822 116 51235	1K	1	MR25	METAL FILM
R 2023	5322 116 55318	511	1	MR25	METAL FILM
R 2024	5322 100 10143	1K	20	0.75W	TRIMMING POTM
R 2026	5322 116 50484	4,64K	1	MR25	METAL FILM
R 2027	5322 116 50484	4,64K	1	MR25	METAL FILM
R 2028	5322 116 50484	4,64K	1	MR25	METAL FILM
R 2029	4822 116 51253	10K	1	MR25	METAL FILM
R 2031	4822 116 51253	10K	1	MR25	METAL FILM
R 2032	5322 116 54655	30,1K	1	MR25	METAL FILM
R 2033	5322 116 50672	51,1K	1	MR25	METAL FILM
R 2036	5322 116 55498	8x4,64K			TRIMMING POTM
R 2037	5322 116 55498	8x4,64K			TRIMMING POTM
R 2038	5322 116 55497	8x10K			TRIMMING POTM
R 2051	4822 116 51253	10K	1	MR25	METAL FILM
R 2052	4822 116 51253	10K	1	MR25	METAL FILM
R 2053	4822 116 51253	10K	1	MR25	METAL FILM
R 2054	4822 116 51253	10K	1	MR25	METAL FILM
R 2056	4822 116 51253	10K	1	MR25	METAL FILM
R 2057	4822 116 51253	10K	1	MR25	METAL FILM
R 2058	4822 116 51253	10K	1	MR25	METAL FILM
R 2059	4822 116 51253	10K	1	MR25	METAL FILM
R 2061	4822 116 51253	10K	1	MR25	METAL FILM
R 2062	5322 116 55497	8x10K			TRIMMING POTM
R 2063	4822 116 51253	10K	1	MR25	METAL FILM
R 2064	4822 116 51253	10K	1	MR25	METAL FILM
R 2066	4822 116 51252	6,81K	1	MR25	METAL FILM
R 2067	5322 116 50484	4,64K	1	MR25	METAL FILM
R 2068	5322 116 55497	8x10K			TRIMMING POTM
R 2071	4822 116 51253	10K	1	MR25	METAL FILM
R 2072	4822 116 51253	10K	1	MR25	METAL FILM
R 2073	5322 116 50484	4,64K	1	MR25	METAL FILM
R 2074	4822 116 51253	10K	1	MR25	METAL FILM
R 2076	4822 116 51268	100K	1	MR25	METAL FILM
R 2077	4822 116 51268	100K	1	MR25	METAL FILM
R 2078	4822 116 51253	10K	1	MR25	METAL FILM
R 2081	4822 116 51253	10K	1	MR25	METAL FILM
R 2082	4822 116 51253	10K	1	MR25	METAL FILM
R 2083	4822 116 51253	10K	1	MR25	METAL FILM
R 2084	5322 116 55419	20,5K	1	MR25	METAL FILM
R 2086	5322 116 55318	511	1	MR25	METAL FILM
R 2087	5322 101 54014	10K	20	0.1W	CARBON POTM LOG + SWIT
R2088					
R2089					
R2090					
R2091					
R 2101	5322 116 55283	402K	1	MR25	METAL FILM
R 2102	5322 116 55364	196K	1	MR25	METAL FILM
R 2103	4822 116 51268	100K	1	MR25	METAL FILM
R 2104	5322 116 54629	14K	1	MR25	METAL FILM
R 2106	5322 116 54716	162K	1	MR25	METAL FILM
R 2107	5322 116 54688	80,6K	1	MR25	METAL FILM
R 2108	5322 116 54716	162K	1	MR25	METAL FILM
R 2109	5322 116 54688	80,6K	1	MR25	METAL FILM
R 2111	5322 116 54716	162K	1	MR25	METAL FILM
R 2112	5322 116 54688	80,6K	1	MR25	METAL FILM

ITEM	ORDERING NUMBER	OHM	TOL (%)	TYPE	REMARKS
R 2113	5322 116 54716	162K	1	MR25	METAL FILM
R 2114	5322 116 54688	80,6K	1	MR25	METAL FILM
R 2116	5322 116 54716	162K	1	MR25	METAL FILM
R 2117	5322 116 54716	162K	1	MR25	METAL FILM
R 2118	5322 116 54469	100	1	MR25	METAL FILM
R 2119	5322 116 54469	100	1	MR25	METAL FILM
R 2121	5322 116 54469	100	1	MR25	METAL FILM
R 2122	5322 116 50679	237	1	MR25	METAL FILM
R 2123	5322 116 50672	51,1K	1	MR25	METAL FILM
R 2124	5322 116 50558	18K7	1	MR25	METAL FILM
R 2126	5322 116 50672	51,1K	1	MR25	METAL FILM
R 2127	5322 116 50508	18K7	1	MR25	METAL FILM
R 2128	4822 116 51266	68,1K	1	MR25	METAL FILM
R 2129	5322 116 54646	23,7K	1	MR25	METAL FILM
R 2130	5322 100 10139	4,7K	20		CERM. POTM
R 2131	5322 116 54497	226	1	MR25	METAL FILM
R 2132	5322 116 50675	2,26K	1	MR25	METAL FILM
R 2133	5322 116 54489	169	1	MR25	METAL FILM
R 2134	5322 116 54587	3,65K	1	MR25	METAL FILM
R 2136	5322 116 54497	226	1	MR25	METAL FILM
R 2137	5322 116 50458	7,87K	1	MR25	METAL FILM
R 2138	5322 116 50904	30,1	1	MR25	METAL FILM
R 2139	5322 116 54606	7,15K	1	MR25	METAL FILM
R 2151	5322 116 54504	274	1	MR25	METAL FILM
R 2152	5322 116 55283	402K	1	MR25	METAL FILM
R 2153	5322 116 55364	196K	1	MR25	METAL FILM
R 2154	4822 116 51268	100K	1	MR25	METAL FILM
R 2156	5322 116 54629	14K	1	MR25	METAL FILM
R 2157	5322 116 54716	162K	1	MR25	METAL FILM
R 2158	5322 116 54688	80,6K	1	MR25	METAL FILM
R 2159	5322 116 54716	162K	1	MR25	METAL FILM
R 2161	5322 116 54688	80,6K	1	MR25	METAL FILM
R 2162	5322 116 54716	162K	1	MR25	METAL FILM
R 2163	5322 116 54688	80,6K	1	MR25	METAL FILM
R 2164	5322 116 54716	162K	1	MR25	METAL FILM
R 2166	5322 116 54688	80,6K	1	MR25	METAL FILM
R 2167	5322 116 54716	162K	1	MR25	METAL FILM
R 2168	5322 116 54716	162K	1	MR25	METAL FILM
R 2169	5322 116 54623	11K	1	MR25	METAL FILM
R 2171	5322 116 50443	12,7K	1	MR25	METAL FILM
R 2172	5322 116 54678	59K	1	MR25	METAL FILM
R 2173	5322 116 54511	316	1	MR25	METAL FILM
R 2174	5322 116 54665	40,2K	1	MR25	METAL FILM
R 2176	4822 116 51253	10K	1	MR25	METAL FILM
R 2177	5322 116 55448	4,02K	1	MR25	METAL FILM
R 2178	4822 116 51284	9,09K	1	MR25	METAL FILM
R 2179	5322 116 54613	8,66K	1	MR25	METAL FILM
R 2181	4822 116 51235	1K	1	MR25	METAL FILM
R 2182	5322 116 54608	7,5K	1	MR25	METAL FILM
R 2183	5322 116 54515	348	1	MR25	METAL FILM

Type	*Ordering code*	*Quantity*
Diodes		
BA182	5322 130 30644	16
BAV21	4822 130 30842	2
BAV45	5322 130 34037	3
BAW62	4822 130 30613	46
BAX12	5322 130 34605	6
BAX12A	5322 130 34605	4
BY206	4822 130 30839	3
BY225 - 200	4822 130 50512	2
BY227	4822 130 34633	4
BY409-A	5322 130 34594	6
BYX49-300	5322 130 34304	1
BYX55-350	4822 130 34275	2
BZX61-C110	5322 130 34671	1
BZX75-C2V8	4822 130 34048	4
BZX75-C3V6	4822 130 30765	2
BZX79-B5V1	4822 130 34233	1
BZX79-B9V1	4822 130 30862	2
BZX79-C36	4822 130 34368	3
BZX79-C5V1	4822 130 34233	2
BZX79-C5V6	4822 130 34173	1
BZX79-C75	5322 130 34442	1
BZX79-C9V1	4822 130 30861	1
OA95	4822 130 30191	3
CQY24A-I (LED)	5322 130 34595	1
Transistors		
BC548C	4822 130 44196	34
BC549C	4822 130 44246	4
BC558B	4822 130 44197	16
BC559B	4822 130 44358	2
BDX77	5322 130 44842	2 (selected pair)
BD237	4822 130 44235	1
BF199	4822 130 44154	6
BF324	4822 130 41448	5
BF338	4822 130 44108	2
BF450	5322 130 44237	12
BFQ10	5322 130 44355	1
BFQ13	5322 130 44404	8
BFS21A	5322 130 40709	2
BFT45	5322 130 44603	2
BSS68	5322 130 44247	1
BSX20	5322 130 40417	1
ON561	5322 130 44643	1

Type	*Ordering number*	*Quantity*
Integrated circuits		
AM9111BPC	5322 209 54584	2
CM215ON	5322 209 86117	1
CA3086	5322 209 84111	1
MBM93419	5322 209 54526	2
HEF40174BP	5322 209 14444	3
HEF4029BP	5322 209 14057	2
HEF4082BP	5322 209 14213	1
N74LS00N	5322 209 84823	1
N74LS02N	5322 209 84312	2
N74LS04N	5322 209 85486	1
N74LS08N	5322 209 84995	1
N74LS132N	5322 209 85201	1
N74LS138N	5322 209 85647	2
N74LS151N	5322 209 85751	1
N74LS190N	5322 209 85491	4
N74LS191N	5322 209 84989	2
N74LS253N	5322 209 85667	4
N74LS32N	5322 209 85311	2
N74S00N	5322 209 84167	3
N74S02N	5322 209 85407	1
N74S10N	5322 209 84954	1
N74S20N	5322 209 85195	1
N74S64N	5322 209 84724	1
N74S74N	5322 209 84183	2
N74S86N	5322 209 85452	1
N82S117N	5322 209 85256	2
NE521N	5322 209 14441	5
N82S09N	5322 209 54526	1
P8085A (μP)	5322 209 86035	4
PROMset programmed	5322 209 14782	1
SN74LS244N	5322 209 86017	3
SN74S373N	5322 209 86062	1
SN74LS374N	5322 209 85869	3
SN74LS74N	5322 209 84183	1
SG3823N	5322 209 84862	2
SL3145C	5322 130 34764	4
Operational Amplifier		
uA741CN	5322 209 85254	1
Transistor Arrays		
SL3145C	5322 130 34764	4
Cathode Ray Tube		
D14-125GH/08	5322 131 24029	1

3.8.3. Miscellaneous parts

Item	*Ordering number*	*Designation*
E1	5322 134 44177	Lamp 28 V - 80 mA
E2	5322 134 44177	Lamp 28 V - 80 mA
F101	4822 252 20017	Thermal fuse (mains trafo)
F201	4822 253 30023	Fuse T 5 x 20, 1.4 A
K501	5322 280 24103	Reed Relay
K601	5322 280 24103	Reed Relay
K1401	5322 280 24103	Reed Relay
L201	5322 281 64154	Coil
L202	5322 281 64154	Coil
L203	5322 281 64154	Coil
L801	5322 156 14074	Coil
L802	5322 156 14074	Coil
L1501	5322 150 14015	Rotary Coil
L2051	5322 152 24092	Coil
S1-S2-S3	5322 276 84076	Push-button switch
S4	See item R3	
S5	See item R4	
S6	5322 273 74011	Attenuator switch without R7
S7	See item R7	
S8	5322 273 74011	Attenuator switch without R8
S9	See item R8	
S10	5322 273 84032	Time base switch without R9
S11	See item R9	
S31, S32	5322 277 14309	Tumbler switch
T101	5322 146 14192	Mains transformer
	4822 252 20017	Thermal fuse for T101
T201	5322 158 34074	Coil assy
T203	5322 148 84047	Converter Transformer
U2	5322 216 54241	Power supply board
U4	5322 218 64056	High voltage unit
U5	5322 216 54245	Amplifier board
U7	5322 320 44029	Delay line unit
U11	5322 216 54235	L.S. Analyzer board
U12	5322 216 54244	D.A. Converter board
U301	5322 216 54243	Attenuator board
U302	5322 105 34034	Attenuator switch (R7, S6, S7) or (R8, S8, R9)
U303	5322 105 34059	Time base switch (R9, S10, S11)

Item	*Ordering number*	*Designation*
X1, X6	5322 264 24015	Calibration terminal
X2, X3, X5, X6	5322 267 10004	H.F. BNC Connector
X4	5322 535 84346	Earthing terminal
X7	4822 265 20051	D.C. input socket with switch
X11, X12, X13, X19, X20	5322 267 64027	P.W. Connector on unit U11
X14	5322 267 64031	P.W. Connector on unit U11
X15, X16, X17	5322 265 54063	L.S. Connector 20-pole on unit U11
X18, X27	5322 268 24116	Coax socket on unit U11
	5322 268 14141	Contact pin for X18 or X27
X21, X22, X23	5322 268 14028	Contact pin on unit U11
X24, X25, X28, X29	5322 265 54006	P.W. connector on unit U12
Plugs	4822 266 30071	3-POLE PLUG
and	4822 265 30121	3-POLE SOCKET
Sockets	4822 266 30072	4-POLE PLUG
	4822 265 30119	4-POLE SOCKET
	4822 266 30073	6-POLE PLUG
	4822 265 30117	6-POLE SOCKET
	4822 266 40057	7-POLE PLUG
	4822 265 40119	7-POLE SOCKET

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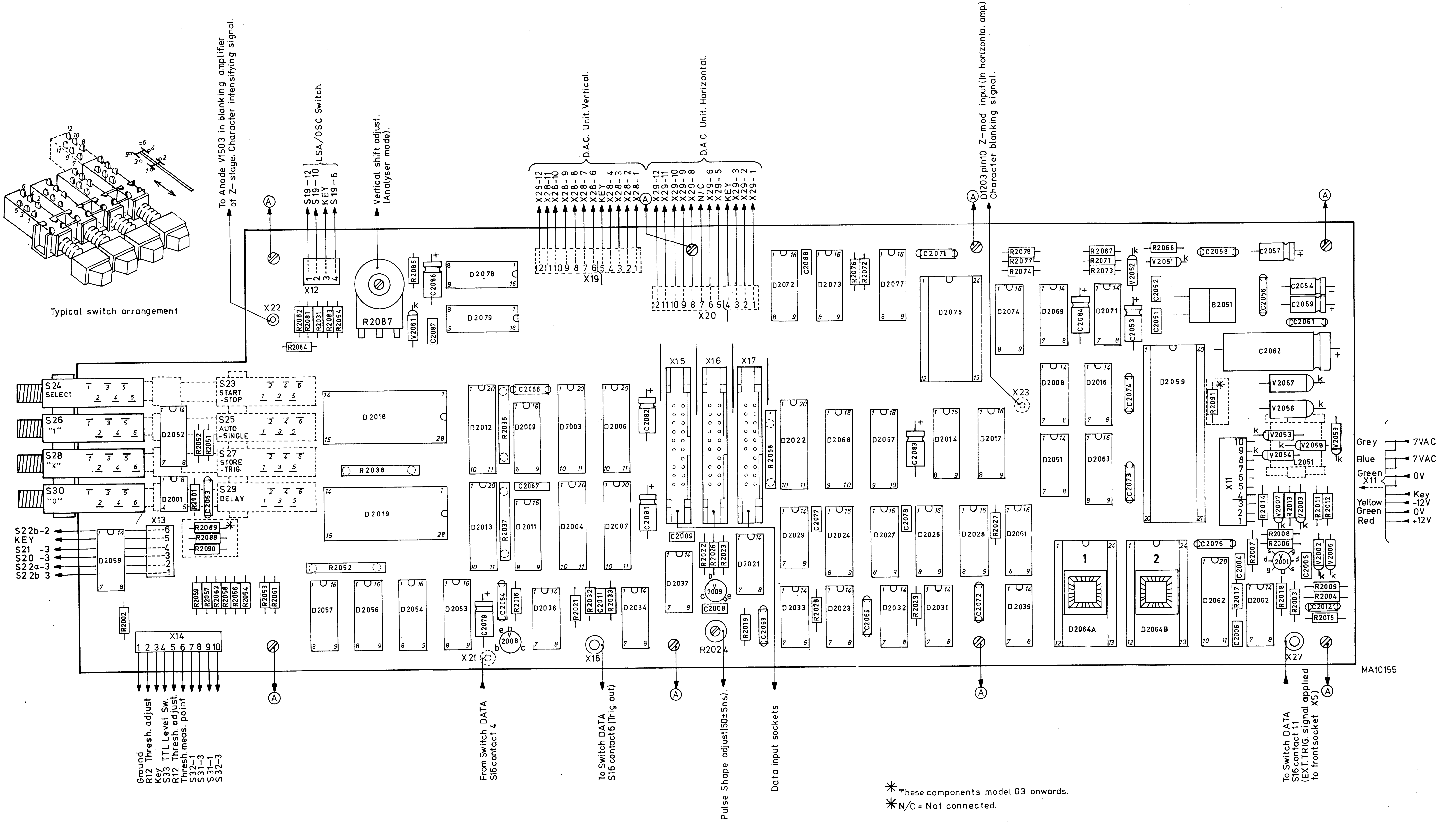
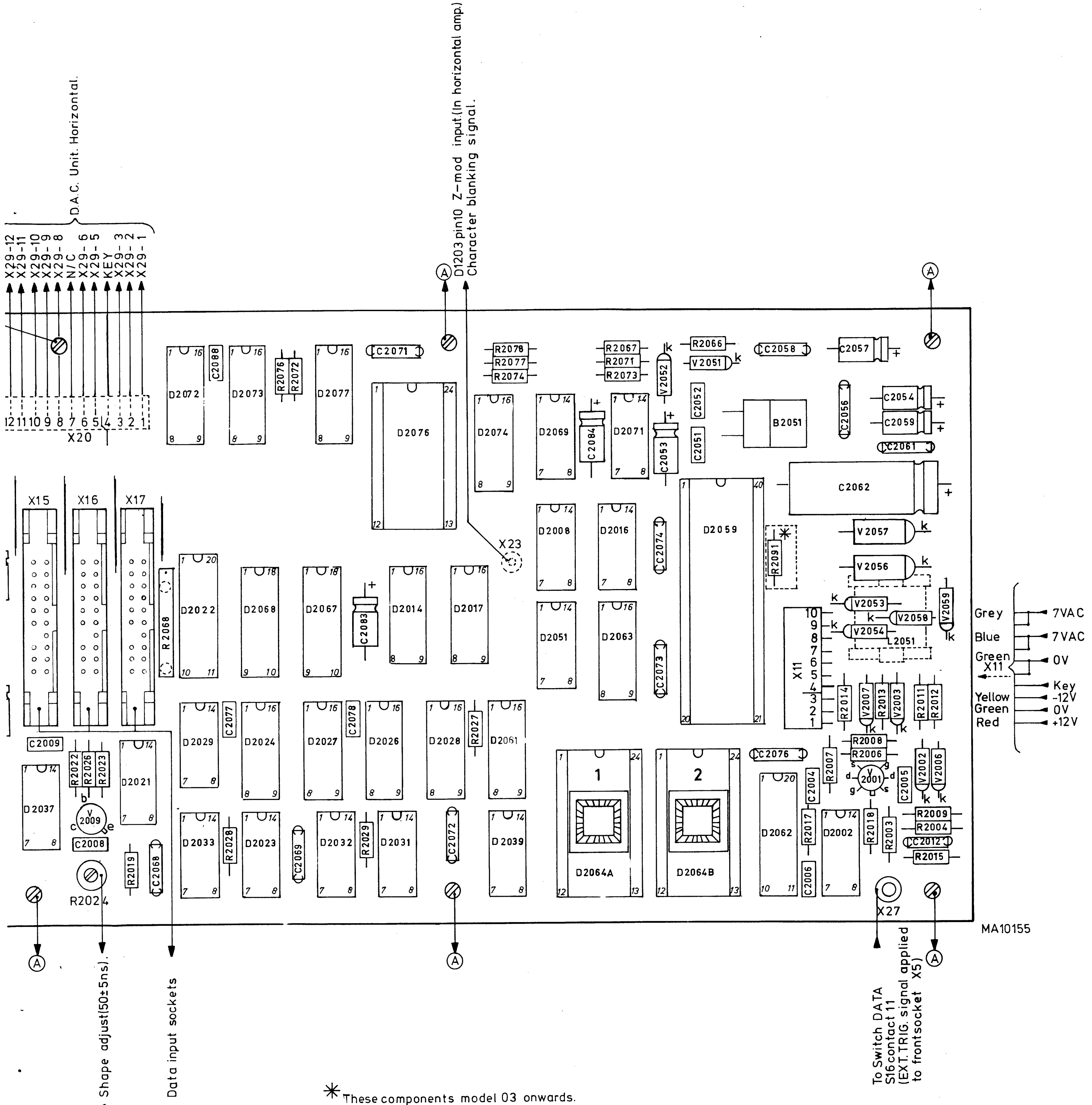

Typical switch arrangement
To Anode V1503 in blanking amplifier of Z-stage. Character intensifying signal.
X22
LSA/OSC Switch.
S19-12
S19-10
KEY
S19-6
X12
Vertical shift adjust. (Analyser mode).
R2087
D.A.C. Unit. Vertical.
X28-12 X28-11 X28-10 X28-9 X28-8 X28-7 X28-6 KEY X28-4 X28-3 X28-2 X28-1
X19
D.A.C. Unit. Horizontal.
X29-12 X29-11 X29-10 X29-9 X29-8 N/C X29-6 X29-5 KEY X29-3 X29-2 X29-1
X20
D1203 pin10 Z-mod input (In horizontal amp.) Character blanking signal.
X23
A
S24 SELECT
S26 "1"
S28 "X"
S30 "0"
S23 START -STOP
S25 AUTO -SINGLE
S27 STORE -TRIG.
S29 DELAY
X13
S22b-2
KEY
S21 -3
S20 -3
S22a-3
S22b 3
X14
1 2 3 4 5 6 7 8 9 10
X15
X16
X17
D2064A
D2064B
1
2
X11
Grey 7VAC
Blue 7VAC
Green 0V
Key
Yellow -12V
Green 0V
Red +12V
X21
X18
R2024
X27
MA10155
Ground
R12 Thresh. adjust
Key
S33 TTL Level Sw.
R12 Thresh. adjust.
Thresh. meas. point
S32-1
S31-3
S31-1
S32-3
From Switch DATA S16 contact 4
To Switch DATA S16 contact 6 (Trig. out)
Pulse Shape adjust (50±5ns).
Data input sockets
To Switch DATA S16 contact 11 (EXT. TRIG. signal applied to frontsocket X5)

*These components model 03 onwards.

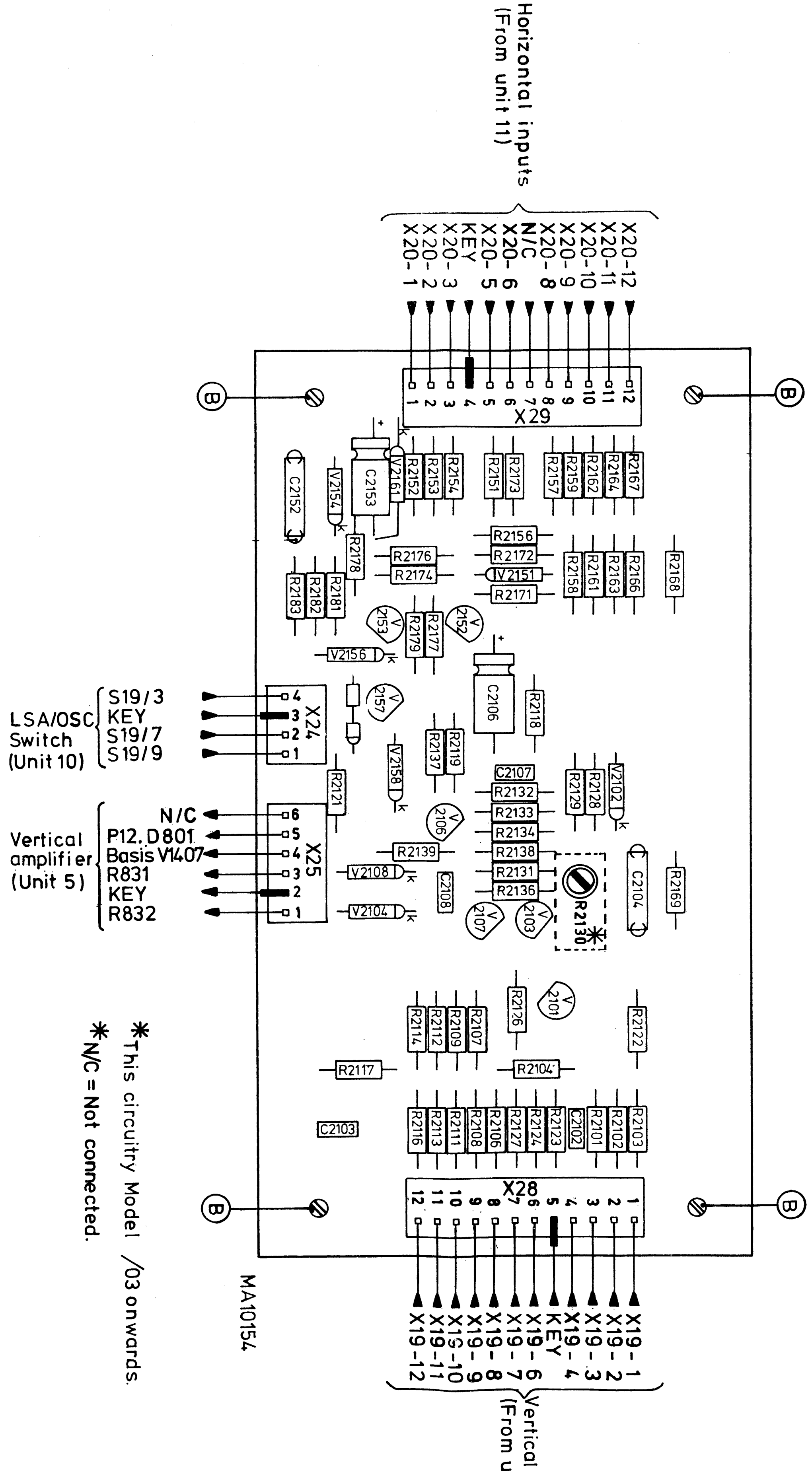
*N/C = Not connected.

Fig. 3.44. Micro-processor p.c. board


D.A.C. Unit. Horizontal.
X29-12
X29-11
X29-10
X29-9
X29-8
N/C
X29-6
X29-5
KEY
X29-3
X29-2
X29-1
X20
D1203 pin10 Z-mod input (In horizontal amp)
Character blanking signal.
X15
X16
X17
X23
X11
Grey
Blue
Green
Yellow
Green
Red
7VAC
7VAC
0V
Key
-12V
0V
+12V
D2076
D2059
D2064A
D2064B
B2051
C2062
X27
R2024
MA10155
Pulse Shape adjust(50±5ns).
Data input sockets
To Switch DATA S16 contact 11 (EXT.TRIG. signal applied to frontsocket X5)

✳ These components model 03 onwards.

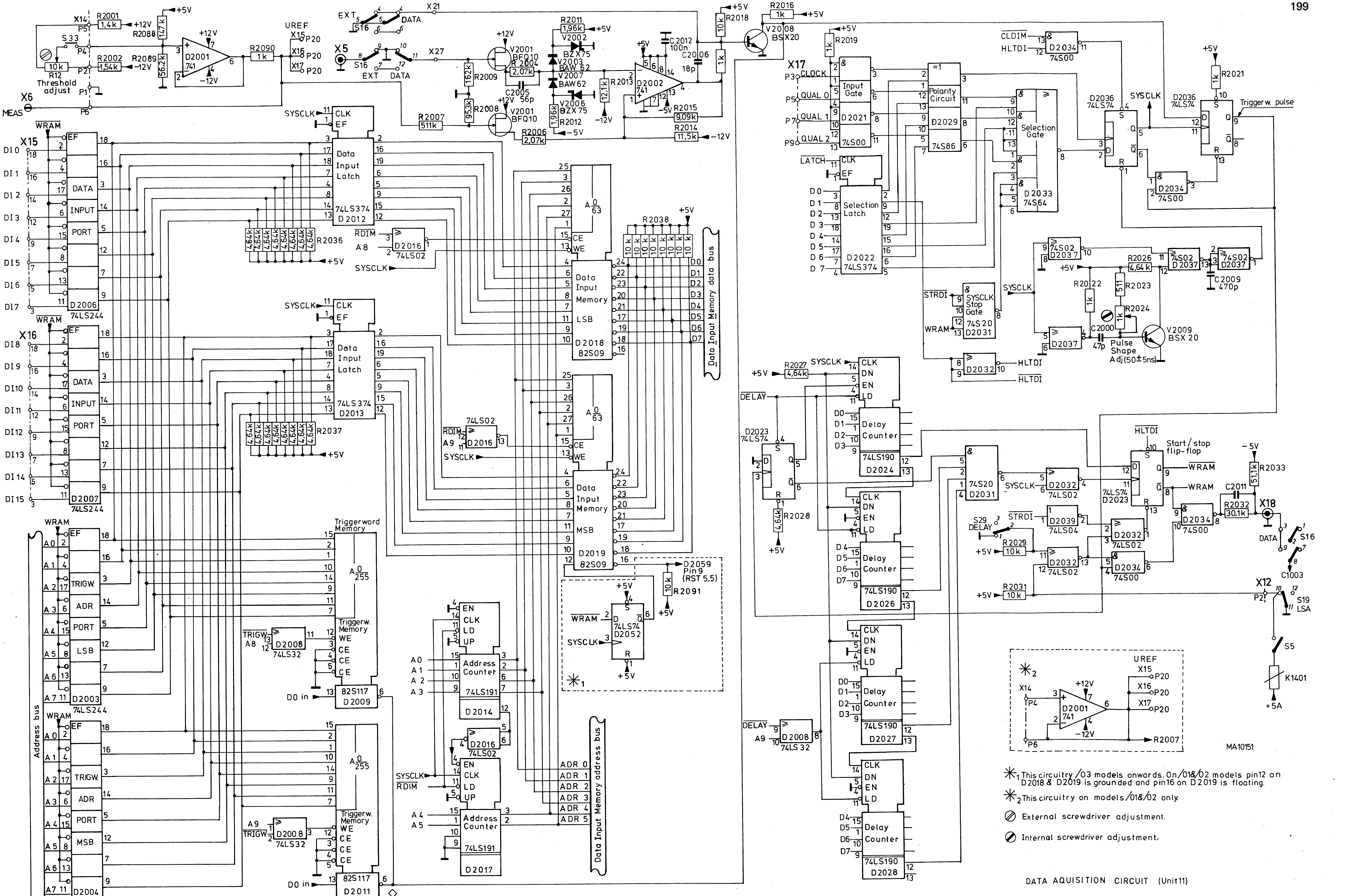
✳ N/C = Not connected.


Horizontal inputs (From unit 11)
X20-12
X20-11
X20-10
X20-9
X20-8
N/C
X20-6
X20-5
KEY
X20-3
X20-2
X20-1
X29
LSA/OSC Switch (Unit 10)
S19/3
KEY
S19/7
S19/9
X24
Vertical amplifier (Unit 5)
N/C
P12. D801
Basis V1407
R831
KEY
R832
X25
R2130
X28
X19-1
X19-2
X19-3
X19-4
KEY
X19-6
X19-7
X19-8
X19-9
X19-10
X19-11
X19-12
Vertical inputs (From unit 11)
MA10154

✳ This circuitry Model /03 onwards.

✳ N/C = Not connected.

Fig. 3.45. DAC p.c. board


Threshold adjust
R12 10k
D2001 741
D2002 741
V2001 BFQ10
V2008 BSX20
X5
X6 MEAS
X14
X15
X16
X17
X18
X12
X21
X27
S16 EXT DATA
UREF
Data Input Latch 74LS374 D2012
Data Input Latch 74LS374 D2013
DATA INPUT PORT D2006 74LS244
DATA INPUT PORT D2007 74LS244
TRIGW. ADR PORT LSB D2003 74LS244
TRIGW. ADR PORT MSB D2004 74LS244
Triggerword Memory A 0/255
Triggerw. Memory 82S117 D2009
Triggerw. Memory 82S117 D2011
Data Input Memory LSB D2018 82S09
Data Input Memory MSB D2019 82S09
Data Input Memory data bus
Data Input Memory address bus
Address bus
Address Counter 74LS191 D2014
Address Counter 74LS191 D2017
Input Gate D2021 74S00
Polarity Circuit D2029 74S86
Selection Gate D2033 74S64
Selection Latch D2022 74LS374
SYSCLK Stop Gate 74S20 D2031
Delay Counter 74LS190 D2024
Delay Counter 74LS190 D2026
Delay Counter 74LS190 D2027
Delay Counter 74LS190 D2028
Start / stop flip-flop
Triggerw. pulse
Pulse Shape Adj(50±5ns)
V2009 BSX 20
K1401
S19 LSA
S5
MA10151

*1 This circuitry /03 models onwards. On/01&/02 models pin12 on D2018 & D2019 is grounded and pin16 on D2019 is floating.

*2 This circuitry on models /01&/02 only.

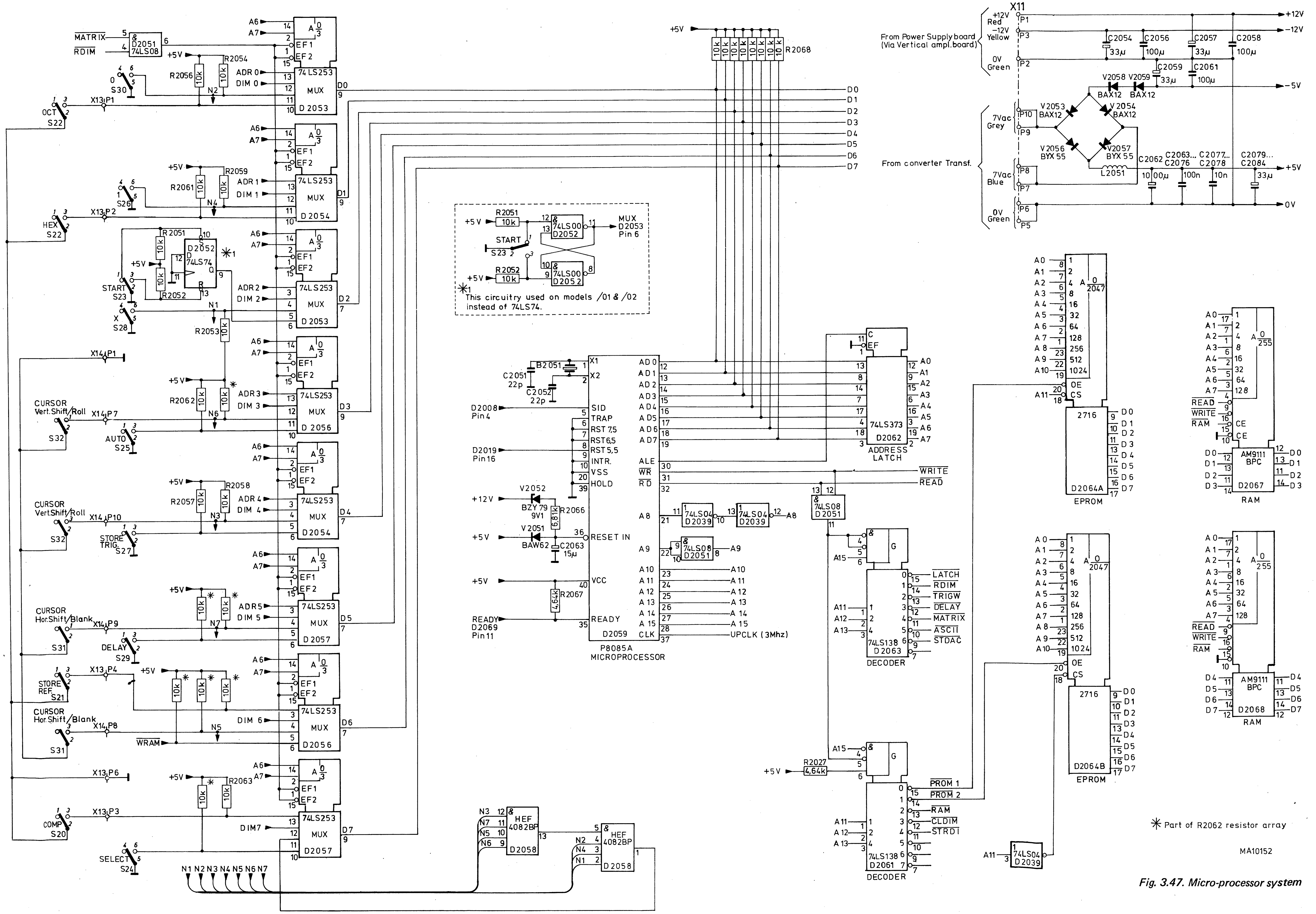
⊘ External screwdriver adjustment.

⊘ Internal screwdriver adjustment.

DATA AQUISITION CIRCUIT (Unit11)

Fig. 3.46. Data aquisition circuit

NOTES:

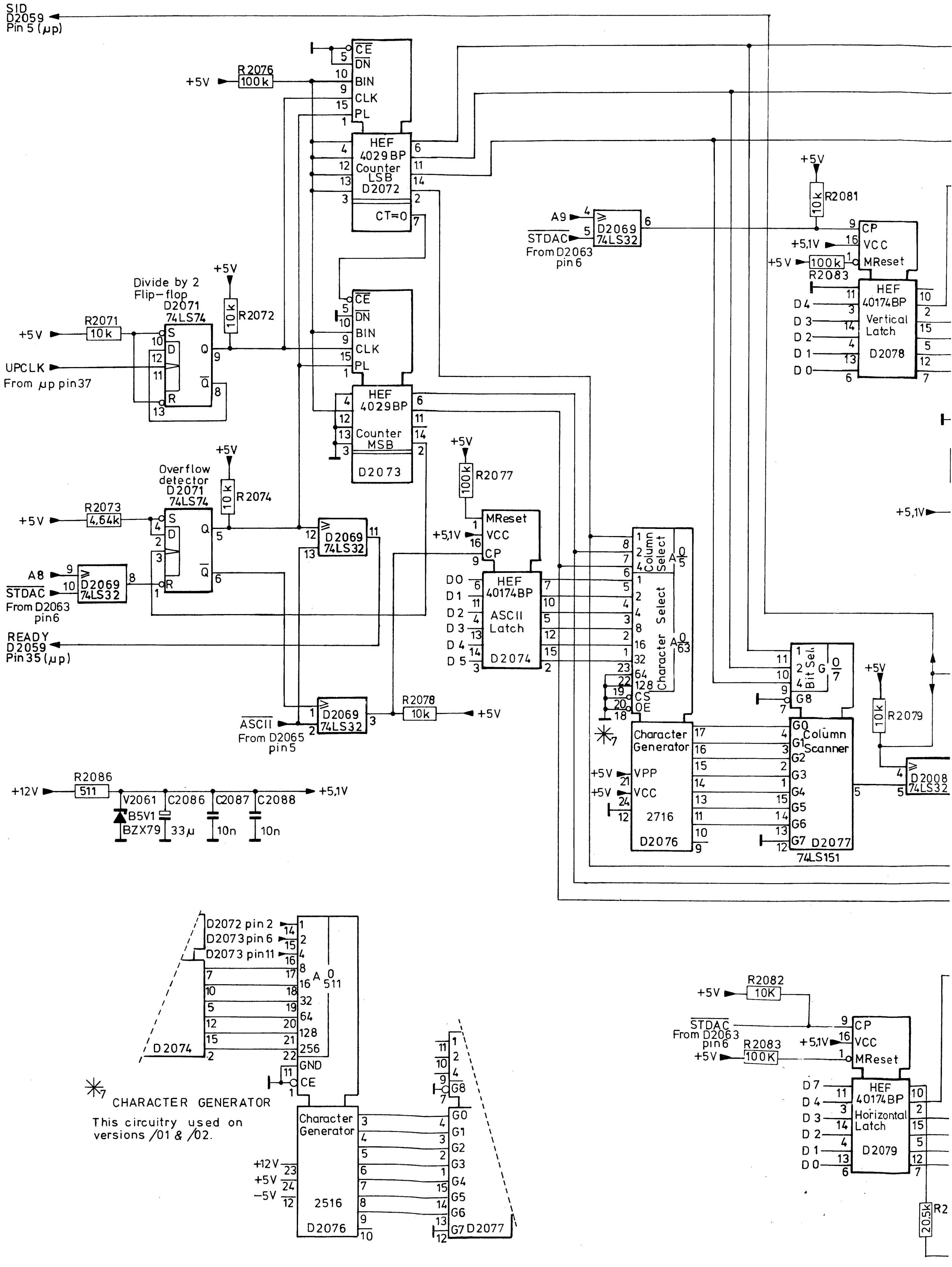

X11
From Power Supply board (Via Vertical ampl. board)
From converter Transf.
+12V
-12V
-5V
+5V
0V
P8085A
MICROPROCESSOR
D2059
74LS373
D2062
ADDRESS LATCH
74LS138
D2063
DECODER
74LS138
D2061
DECODER
2716
D2064A
EPROM
2716
D2064B
EPROM
AM9111 BPC
D2067
RAM
AM9111 BPC
D2068
RAM
74LS253
MUX
D2053
D2054
D2056
D2057
74LS08
D2051
74LS74
D2052
74LS00
74LS04
D2039
HEF 4082BP
D2058
START
S23
OCT
S22
HEX
CURSOR Vert.Shift/Roll
S32
AUTO
S25
STORE TRIG.
S27
CURSOR Hor.Shift/Blank
S31
DELAY
S29
STORE REF.
S21
COMP
S20
SELECT
S24
MATRIX
RDIM
WRAM
LATCH
RDIM
TRIGW
DELAY
MATRIX
ASCII
STDAC
PROM 1
PROM 2
RAM
CLDIM
STRDI
WRITE
READ
UPCLK (3Mhz)
READY D2069 Pin11
D2008 Pin4
D2019 Pin16
R2068
R2027
V2052 BZY79 9V1
V2051 BAW62
B2051
C2051 22p
C2052 22p
V2053 BAX12
V2054 BAX12
V2056 BYX55
V2057 BYX55
V2058 BAX12
V2059 BAX12
L2051
This circuitry used on models /01 & /02 instead of 74LS74.
MA10152

✱ Part of R2062 resistor array

Fig. 3.47. Micro-processor system

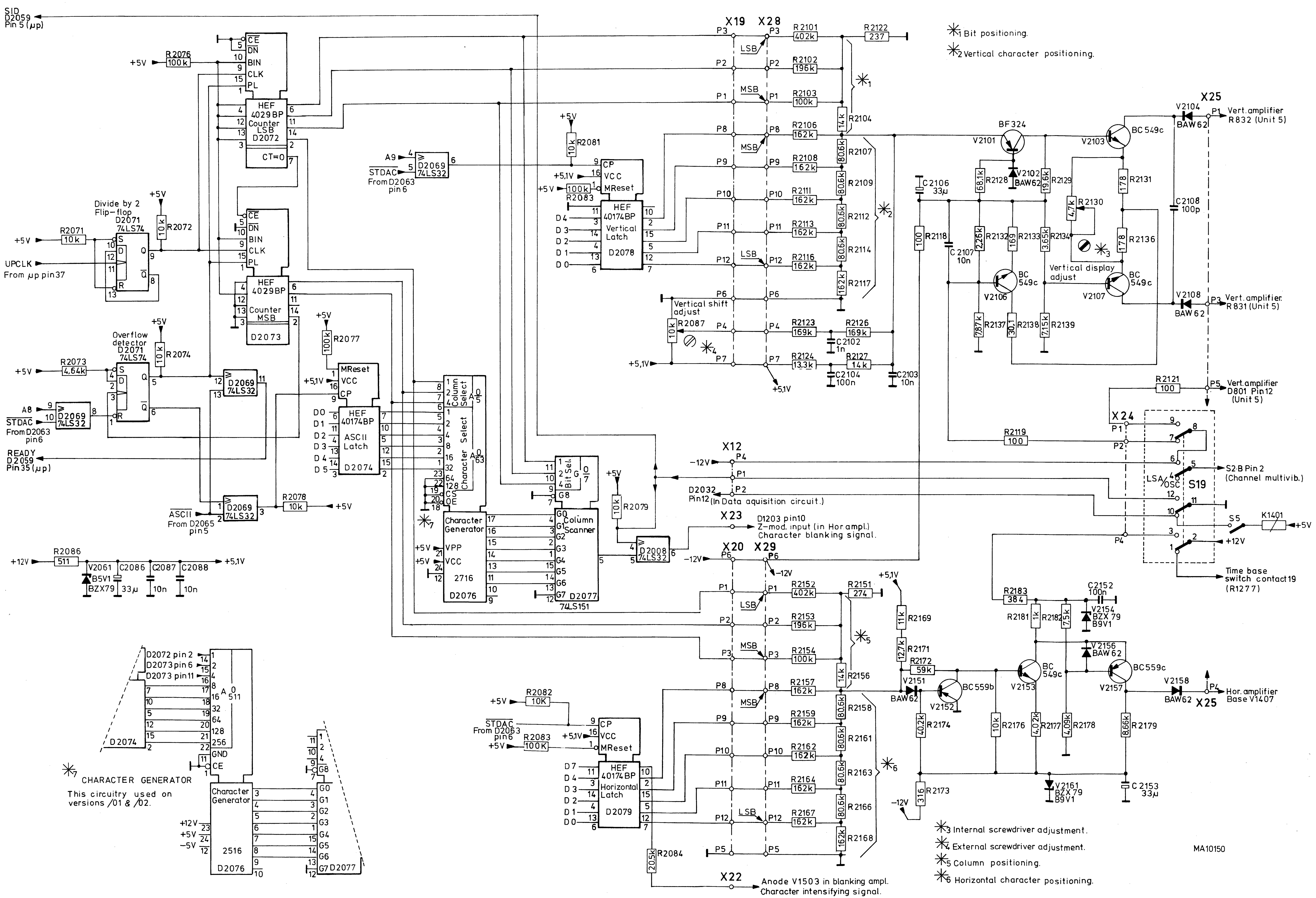
NOTES:

NOTES:


SID D2059 Pin 5 (µp)
+5V
R2076 100k
CE DN BIN CLK PL
HEF 4029BP Counter LSB D2072
CT=0
HEF 4029BP Counter MSB D2073
Divide by 2 Flip-flop D2071 74LS74
R2071 10k
R2072 10k
UPCLK From µp pin37
Overflow detector D2071 74LS74
R2073 4,64k
R2074 10k
A8
STDAC From D2063 pin6
D2069 74LS32
READY D2059 Pin35 (µp)
ASCII From D2065 pin5
R2078 10k
R2077 100k
MReset VCC CP
HEF 40174BP ASCII Latch D2074
D0 D1 D2 D3 D4 D5
+5,1V
A9
STDAC From D2063 pin6
R2081 10k
R2083 100k
HEF 40174BP Vertical Latch D2078
Column Select
Character Select
A0 5
A0 63
CS OE
Character Generator 2716 D2076
VPP VCC
Bit Sel.
G 0 7
G8
Column Scanner D2077 74LS151
G0 G1 G2 G3 G4 G5 G6 G7
R2079 10k
D2008 74LS32
R2086 511
+12V
V2061 B5V1 BZX79
C2086 33µ
C2087 10n
C2088 10n
+5,1V
D2072 pin 2
D2073 pin 6
D2073 pin 11
D2074
A 0 511
GND
CE
Character Generator 2516 D2076
+12V +5V −5V
R2082 10K
STDAC From D2063 pin6
R2083 100K
HEF 40174BP Horizontal Latch D2079
D7 D4 D3 D2 D1 D0
20,5k R2

✳7 CHARACTER GENERATOR

This circuitry used on versions /01 & /02.


SID D2059 Pin 5 (µp)
+5V R2076 100k
CE DN BIN CLK PL
HEF 4029BP Counter LSB D2072
CT=0
Divide by 2 Flip-flop D2071 74LS74
+5V R2071 10k
UPCLK From µp pin37
R2072 10k
HEF 4029BP Counter MSB D2073
Overflow detector D2071 74LS74
+5V R2073 4.64k
R2074 10k
D2069 74LS32
A8 STDAC From D2063 pin6
READY D2059 Pin35 (µp)
ASCII From D2065 pin5
R2078 10k +5V
+12V R2086 511 V2061 B5V1 BZX79 C2086 33µ C2087 10n C2088 10n +5,1V
A9 STDAC From D2063 pin 6 D2069 74LS32
+5V R2077 100k
MReset VCC CP
HEF 40174BP ASCII Latch D2074
D0 D1 D2 D3 D4 D5
Column Select A0 A5
Character Select A0 A63
CS OE
Character Generator
VPP VCC 2716 D2076
Bit Sel. G0 G7 G8
Column Scanner D2077 74LS151
+5V R2081 10k
HEF 40174BP Vertical Latch D2078
R2083 100k
R2079 10k
D2008 74LS32
X19 X28
P3 P2 P1 P8 P9 P10 P11 P12 P6 P4 P7
LSB MSB
R2101 402k R2102 196k R2103 100k R2106 162k R2108 162k R2111 162k R2113 162k R2116 162k
R2122 237
R2104 14k R2107 80.6k R2109 80.6k R2112 80.6k R2114 80.6k R2117 162k
Vertical shift adjust R2087 10k
R2123 169k R2126 169k C2102 1n
R2124 13.3k R2127 14k C2104 100n C2103 10n
+5,1V
C2106 33µ R2118 100 C2107 10n
BF324 V2101 V2102 BAW62 R2128 68.1k R2129 19.6k
BC549c V2103 R2131 178 R2130 4.7k R2136 178
R2132 2.26k R2133 169 R2134 3.65k
BC 549c V2106 BC 549c V2107
Vertical display adjust
R2137 7.87k R2138 30.1 R2139 7.15k
V2104 BAW62 X25 P1 Vert.amplifier R832 (Unit 5)
C2108 100p
V2108 BAW62 P3 Vert.amplifier R831 (Unit 5)
R2121 100 P5 Vert.amplifier D801 Pin12 (Unit 5)
X24 P1 P2 P4
R2119 100
X12 −12V P4 P1 P2
D2032 Pin12 (In Data aquisition circuit.)
X23 D1203 pin10 Z-mod. input (in Hor.ampl.) Character blanking signal.
S2:B Pin 2 (Channel multivib.)
LSA/OSC S19
S5 K1401 +5V
+12V
Time base switch contact 19 (R1277)
X20 X29 P6 −12V
R2152 402k R2151 274 R2153 196k R2154 100k R2157 162k R2159 162k R2162 162k R2164 162k R2167 162k
R2156 14k R2158 80.6k R2161 80.6k R2163 80.6k R2166 80.6k R2168 162k
P5
+5V R2082 10K
STDAC From D2063 pin6
R2083 100K
HEF 40174BP Horizontal Latch D2079
D7 D4 D3 D2 D1 D0
R2084 20.5k
X22 Anode V1503 in blanking ampl. Character intensifying signal.
+5,1V R2169 11k R2171 12.7k R2172 59k
V2151 BAW62 BC559b V2152
R2174 40.2k R2173 316 −12V
R2183 384 C2152 100n R2181 1k R2182 7.5k V2154 BZX79 B9V1
V2156 BAW62
BC 549c V2153 BC559c V2157
R2176 10k R2177 4.02k R2178 4.09k R2179 8.66k
V2161 BZX79 B9V1 C2153 33µ
V2158 BAW62 X25 P4 Hor.amplifier Base V1407
D2072 pin 2 D2073 pin 6 D2073 pin 11 D2074
A0 A511
GND CE
Character Generator
+12V +5V −5V 2516 D2076
G0 G1 G2 G3 G4 G5 G6 G7 G8 D2077
MA10150

*1 Bit positioning.

*2 Vertical character positioning.

*3 Internal screwdriver adjustment.

*4 External screwdriver adjustment.

*5 Column positioning.

*6 Horizontal character positioning.

*7 CHARACTER GENERATOR

This circuitry used on versions /01 & /02.

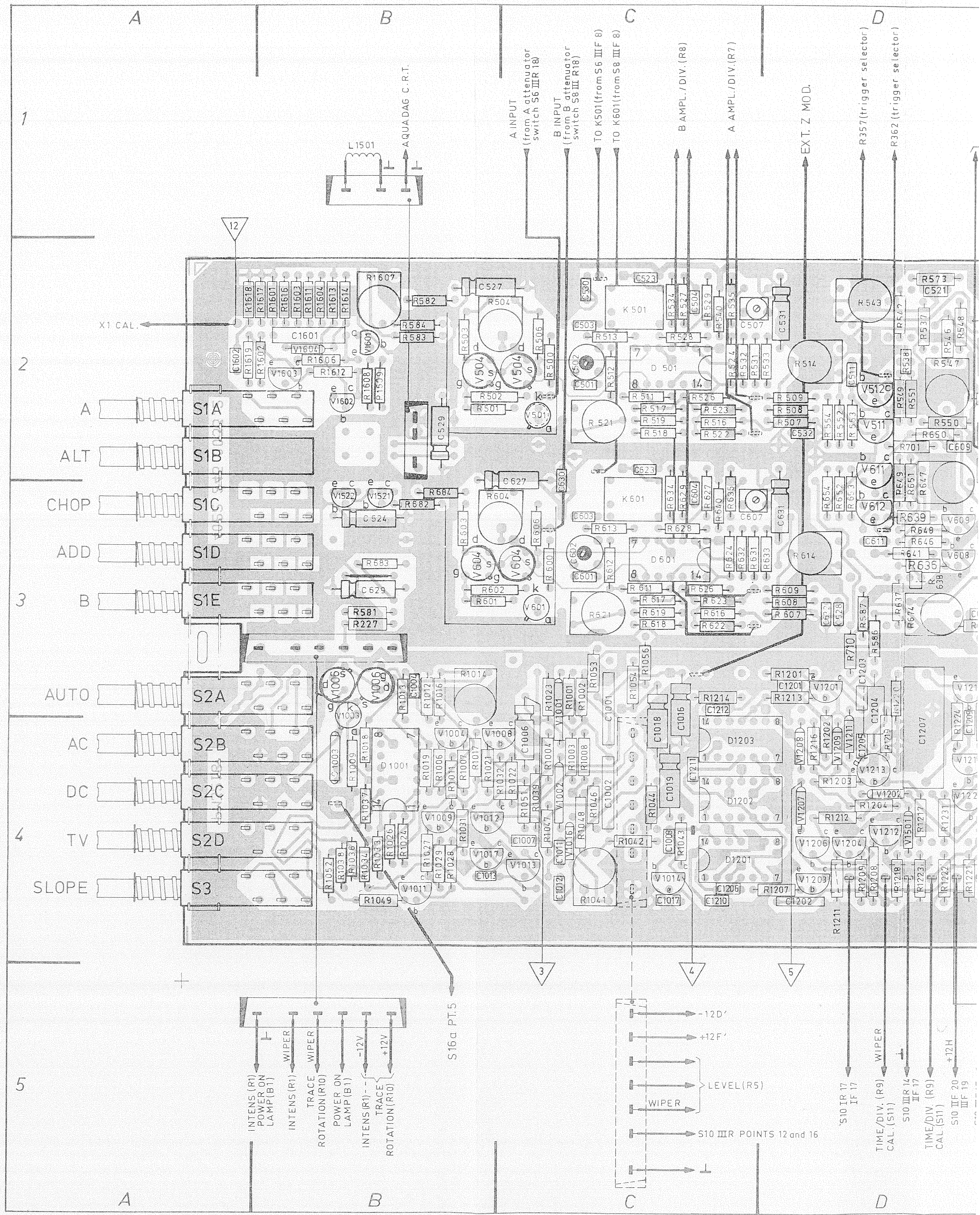
Fig. 3.48. Display circuit

3.9. LOCATION LIST (of components on the amplifier board)

Item	*Grid Loc.*
C101	Rear panel
C200	Power supply
C201	Power supply
C202	Power supply
C203	Power supply
C204	Power supply
C206	Power supply
C207	Power supply
C208	Power supply
C209	Power supply
C211	Power supply
C212	High tension unit
C213	
C214	
C216	
C217	
C218	Power supply
C219	Power supply
C221	Power supply
C222	Power supply
C223	Power supply
C224	Power supply
C226	Power supply
C227	Power supply
C228	Power supply
C229	Power supply
C231	Power supply
C301	Att. unit
C305	Att. unit
C307	Att. unit
C308	Att. unit
C309	Att. unit
C310	Att. unit
C311	Att. unit
C312	Att. unit
C313	Att. unit
C314	Att. unit
C315	Att. unit
C316	Att. unit
C317	Att. unit
C318	Att. unit
C319	Att. unit
C320	Att. unit
C321	Att. unit
C322	Att. unit
C324	Att. unit
C351	Att. unit
C352	Att. unit
C353	Att. unit
C354	Att. unit
C356	Att. unit
C357	Att. unit
C358	Att. unit
C401	Att. unit
C405	Att. unit
C407	Att. unit
C408	Att. unit
C409	Att. unit
C410	Att. unit
C411	Att. unit
C412	Att. unit
C413	Att. unit
C414	Att. unit
C415	Att. unit
C416	Att. unit
C417	Att. unit
C418	Att. unit
C419	Att. unit
C420	Att. unit
C421	Att. unit
C422	Att. unit
C424	Att. unit
C501	C-2
C502	C-2
C504	D-2
C507	D-2
C508	D-2
C509	D-2
C511	D-2
C512	E-2
C513	E-2
C514	E-2
C517	E-2
C518	E-2
C519	E-2
C521	D-2
C522	E-2
C523	C-2
C524	B-3
C526	C-2
C527	B-2/C-2
C528	D-3
C529	B-2
C531	C-2
C601	C-3
C602	C-3
C604	D-3
C607	D-2/D-3
C608	D-3
C609	D-2
C611	D-3
C612	D-3
C613	D-3
C614	D-3
C616	E-3
C617	E-3
C618	E-3
C619	E-3
C621	E-3
C622	E-2/E-3
C623	C-3
C627	B-2/C-2
C629	B-3
C631	C-3
C701	D-2
C702	E-2
C703	E-2
C704	E-2
C705	E-2
C706	D-2
C707	E-2
C801	E-3
C802	E-3
C803	E-3
C804	F-3
C805	F-2
C806	F-3
C807	E-3
C808	F-3
C809	F-3
C810	F-2
C811	F-3
C813	F-3
C814	F-2
C815	F-3
C816	F-2
C818	F-2
C819	F-2
C821	F-2
C1001	C-3/C-4
C1002	C-4
C1003	B-4
C1004	B-3
C1006	C-3/C-4
C1007	C-4
C1008	C-4
C1011	C-4
C1012	C-4
C1013	B-4
C1016	C-3/C-4
C1017	C-4
C1018	C-3/C-4
C1019	C-4
C1201	D-3
C1202	D-4
C1203	D-3
C1204	D-3/D-4
C1205	D-4
C1206	C-4
C1207	D-3/D-4
C1208	E-3/E-4
C1209	D-3/D-4
C1210	C-4
C1211	C-4
C1212	C-3
C1213	E-4
C1214	E-4
C1216	E-3/E-4
C1401	E-4
C1402	E-4
C1403	E-4
C1404	F-3
C1406	G-3
C1407	F-3/G-3
C1408	F-3
C1409	F-3/G-3
C1411	F-2/G-2
C1412	F-2/G-2
C1413	F-2/G-2
C1414	G-3
C1416	G-2
C1417	G-2
C1418	G-2
C1419	F-3
C1421	F-2
C1501	E-4
C1502	F-4
C1503	F-4
C1504	. .
C1506	F-4
C1507	F-4
C1508	F-4
C1509	F-4/G-4
C1511	F-4
C1512	F-4/G-4
C1513	On Tube
C1601	B-2
C1602	A-2
R1	Front panel
R2	
R3	
R4	
R5	
R6	
R7	
R8	
R9	
R10	
R11	
R200	Power supply
R201	Power supply
R202	Power supply
R203	Power supply
R204	Power supply
R206	Power supply
R207	Power supply
R208	Power supply
R209	Power supply
R210	Power supply
R211	High t. u.
R212	Power supply
R227	B-3
R302	Att. unit
R303	On switch S6
R304	On switch S6
R306	
R307	Att. unit
R308	Att. unit
R309	Att. unit
R311	Att. unit
R312	Att. unit
R313	On switch S6
R314	
R316	Att. unit
R317	Att. unit
R318	Att. unit
R319	Att. unit
R354	Att. unit
R356	Att. unit
R357	Att. unit
R358	Att. unit
R359	Att. unit
R361	Att. unit
R362	Att. unit
R363	Att. unit
R364	Att. unit
R366	Att. unit
R367	Att. unit
R369	Att. unit
R371	Att. unit
R372	Att. unit
R373	Att. unit
R402	Att. unit
R403	On switch S8
R404	
R406	
R407	Att. unit
R408	Att. unit
R409	Att. unit
R411	Att. unit
R412	Att. unit
R413	On switch S8
R414	
R416	Att. unit
R417	Att. unit
R418	Att. unit
R419	Att. unit
R500	C-2
R501	B-2/C-2
R502	B-2/C-2
R503	C-2
R504	B-2/C-2
R506	B-2
R507	C-2
R508	C-2
R509	C-2
R511	C-2
R512	C-2
R513	C-2
R514	C-2
R516	C-2
R517	C-2
R518	C-2
R519	C-2
R521	C-2/D-2
R522	C-2/D-2
R523	C-2/D-2
R524	D-2
R526	C-2/D-2
R527	C-2/D-2
R528	C-2
R529	C-2/D-2
R531	C-2/D-2
R532	D-2
R533	D-2
R534	D-2
R536	D-2
R537	D-2
R538	D-2
R539	D-2
R541	D-2
R542	D-2
R543	D-2
R544	D-2
R546	D-2
R547	D-2
R548	D-2
R549	D-2
R550	D-2
R551	D-2
R552	D-2
R553	D-2
R554	D-2
R556	E-2
R557	E-2
R558	E-2
R559	E-2
R567	E-2
R568	E-2
R569	E-2
R571	E-2
R572	E-2
R573	D-2
R577	E-2
R581	B-3
R582	B-2
R583	B-2
R584	C-2
R586	D-3
R587	D-3
R600	C-3
R601	B-3/C-3
R602	B-3/C-3
R603	C-3
R604	B-3/C-3
R606	B-3
R607	C-3
R608	C-3
R609	C-3
R611	C-3
R612	C-3
R613	C-3
R614	C-3
R616	C-3
R617	C-2
R618	C-3
R619	C-2/C-3
R621	C-3/D-3
R622	C-3/D-3
R623	C-3/D-3
R624	D-3
R626	C-3/D-3
R627	C-3/D-3
R628	C-3
R629	C-3/D-3
R631	C-3/D-3
R632	D-3
R633	D-3
R634	D-3
R636	D-3
R637	D-3
R638	D-3
R639	D-3
R641	D-3
R644	D-3
R646	D-3
R647	D-2/D-3
R648	D-3
R649	D-2/D-3
R650	D-2
R651	D-2/D-3
R652	D-2/D-3
R653	D-2/D-3
R654	D-2/D-3
R656	D-3
R657	D-3
R658	D-3
R659	E-3
R661	E-3
R662	E-3
R663	E-3
R664	E-3
R666	E-3
R667	E-3
R668	E-3
R669	E-3
R671	E-3
R672	E-3
R673	E-3
R674	D-3
R676	D-3
R677	E-2
R682	B-3
R683	B-3
R684	C-3
R701	D-2
R702	E-2
R703	E-2
R704	E-2
R705	E-3
R706	D-2/E-2
R707	D-2
R708	D-2
R709	E-2
R710	D-3
R711	E-2/E-3
R712	E-2
R713	E-3
R714	E-2
R716	E-2/E-3
R717	E-3
R801	E-2
R802	E-3
R803	E-2/E-3
R804	E-2
R806	E-3
R807	E-3
R808	E-2
R809	E-2
R811	E-3/F-3
R812	F-3
R813	F-3
R814	E-3
R816	E-2/E-3
R817	F-3
R818	E-2
R819	F-3
R821	F-3
R822	F-3
R823	F-3
R824	F-2/F-3
R825	F-3
R826	F-2/F-3
R827	F-3
R828	F-3
R829	F-3
R831	F-2
R832	F-2
R833	F-2
R837	F-2
R838	F-2
R839	F-2
R841	F-2
R842	F-2
R843	F-2
R844	F-2
R846	F-2
R847	F-2
R848	F-2
R849	F-2
R851	F-2
R852	F-2
R853	F-2
R854	E-2
R856	E-2
R857	E-2
R858	E-2/F-2
R859	F-2
R861	E-2
R862	F-2
R863	E-2
R1001	C-3
R1002	C-3
R1003	C-4
R1004	C-4
R1005	B-4
R1006	B-4
R1007	B-4
R1008	C-4
R1009	B-4
R1011	B-4
R1012	B-3
R1013	B-3
R1014	B-3
R1016	B-3
R1017	B-4
R1018	B-4
R1019	B-4
R1021	B-4
R1022	C-4
R1023	C-3
R1024	B-4
R1026	B-4
R1027	B-4
R1028	B-4
R1029	B-4
R1031	B-4
R1032	B-4/C-4
R1033	B-4
R1034	B-4
R1036	B-4
R1037	B-4
R1038	B-4
R1039	C-4
R1041	C-4
R1042	C-4
R1043	C-4
R1044	C-4
R1046	C-4
R1047	C-4
R1048	C-4
R1049	B-4
R1051	C-4
R1052	B-4
R1053	C-3
R1054	C-3
R1056	C-3
R1201	D-3
R1202	D-4
R1203	D-4
R1204	D-4
R1207	D-4
R1208	D-4
R1209	D-4
R1211	D-4
R1212	D-4
R1213	D-3
R1214	C-3
R1216	D-4
R1217	D-4
R1218	D-4
R1219	D-4
R1221	D-4
R1222	D-4
R1223	D-4
R1224	D-3/D-4
R1226	D-3/D-4
R1227	D-4
R1228	E-3/E-4
R1229	D-4
R1231	D-4
R1232	E-4
R1233	E-4
R1234	E-4
R1236	D-4
R1237	E-3
R1238	E-3
R1239	E-3
R1276	On switch S10
R1277	
R1278	
R1279	
R1281	
R1282	
R1283	
R1284	
R1286	
R1287	
R1288	
R1289	
R1401	E-4
R1402	E-4
R1403	E-4
R1404	E-4
R1406	E-4
R1407	E-4
R1408	E-4
R1409	E-4
R1411	E-4
R1412	E-4

Item	*Grid Loc.*
R516	C-2
R517	C-2
R518	C-2
R519	C-2
R521	C-2/D-2
R522	C-2/D-2
R523	C-2/D-2
R524	D-2
R526	C-2/D-2
R527	C-2/D-2
R528	C-2
R529	C-2/D-2
R531	C-2/D-2
R532	D-2
R533	D-2
R534	D-2
R536	D-2
R537	D-2
R538	D-2
R539	D-2
R541	D-2
R542	D-2
R543	D-2
R544	D-2
R546	D-2
R547	D-2
R548	D-2
R549	D-2
R550	D-2
R551	D-2
R552	D-2
R553	D-2
R554	D-2
R556	E-2
R557	E-2
R558	E-2
R559	E-2
R567	E-2
R568	E-2
R569	E-2
R571	E-2
R572	E-2
R573	D-2
R577	E-2
R581	B-3
R582	B-2
R583	B-2
R584	C-2
R586	D-3
R587	D-3
R600	C-3
R601	B-3/C-3
R602	B-3/C-3
R603	C-3
R604	B-3/C-3
R606	B-3
R607	C-3
R608	C-3
R609	C-3
R611	C-3
R612	C-3
R613	C-3
R614	C-3
R616	C-3
R617	C-2
R618	C-3
R619	C-2/C-3
R621	C-3/D-3
R622	C-3/D-3
R623	C-3/D-3
R624	D-3
R626	C-3/D-3
R627	C-3/D-3
R628	C-3
R629	C-3/D-3
R631	C-3/D-3
R632	D-3
R633	D-3
R634	D-3
R636	D-3
R637	D-3
R638	D-3
R639	D-3
R641	D-3
R644	D-3
R646	D-3
R647	D-2/D-3
R648	D-3
R649	D-2/D-3
R650	D-2
R651	D-2/D-3
R652	D-2/D-3
R653	D-2/D-3
R654	D-2/D-3
R656	D-3
R657	D-3
R658	D-3
R659	E-3
R661	E-3
R662	E-3
R663	E-3
R664	E-3
R666	E-3
R667	E-3
R668	E-3
R669	E-3
R671	E-3
R672	E-3
R673	E-3
R674	D-3
R676	D-3
R677	E-2
R682	B-3
R683	B-3
R684	C-3
R701	D-2
R702	E-2
R703	E-2
R704	E-2
R705	E-3
R706	D-2/E-2
R707	D-2
R708	D-2
R709	E-2
R710	D-3
R711	E-2/E-3
R712	E-2
R713	E-3
R714	E-2
R716	E-2/E-3
R717	E-3
R801	E-2
R802	E-3
R803	E-2/E-3
R804	E-2
R806	E-3
R807	E-3
R808	E-2
R809	E-2
R811	E-3/F-3
R812	F-3
R813	F-3
R814	E-3
R816	E-2/E-3
R817	F-3
R818	E-2
R819	F-3
R821	F-3
R822	F-3
R823	F-3
R824	F-2/F-3
R825	F-3
R826	F-2/F-3
R827	F-3
R828	F-3
R829	F-3
R831	F-2
R832	F-2
R833	F-2
R837	F-2
R838	F-2
R839	F-2
R841	F-2
R842	F-2
R843	F-2
R844	F-2
R846	F-2
R847	F-2
R848	F-2
R849	F-2
R851	F-2
R852	F-2
R853	F-2
R854	E-2
R856	E-2
R857	E-2
R858	E-2/F-2
R859	F-2
R861	E-2
R862	F-2
R863	E-2
R1001	C-3
R1002	C-3
R1003	C-4
R1004	C-4
R1005	B-4
R1006	B-4
R1007	B-4
R1008	C-4
R1009	B-4
R1011	B-4
R1012	B-3
R1013	B-3
R1014	B-3
R1016	B-3
R1017	B-4
R1018	B-4
R1019	B-4
R1021	B-4
R1022	C-4
R1023	C-3
R1024	B-4
R1026	B-4
R1027	B-4
R1028	B-4
R1029	B-4
R1031	B-4
R1032	B-4/C-4
R1033	B-4
R1034	B-4
R1036	B-4
R1037	B-4
R1038	B-4
R1039	C-4
R1041	C-4
R1042	C-4
R1043	C-4
R1044	C-4
R1046	C-4
R1047	C-4
R1048	C-4
R1049	B-4
R1051	C-4
R1052	B-4
R1053	C-3
R1054	C-3
R1056	C-3
R1201	D-3
R1202	D-4
R1203	D-4
R1204	D-4
R1207	D-4
R1208	D-4
R1209	D-4
R1211	D-4
R1212	D-4
R1213	D-3
R1214	C-3
R1216	D-4
R1217	D-4
R1218	D-4
R1219	D-4
R1221	D-4
R1222	D-4
R1223	D-4
R1224	D-3/D-4
R1226	D-3/D-4
R1227	D-4
R1228	E-3/E-4
R1229	D-4
R1231	D-4
R1232	E-4
R1233	E-4
R1234	E-4
R1236	D-4
R1237	E-3
R1238	E-3
R1239	E-3
R1276	On switch S10
R1277	
R1278	
R1279	
R1281	
R1282	
R1283	
R1284	
R1286	
R1287	
R1288	
R1289	
R1401	E-4
R1402	E-4
R1403	E-4
R1404	E-4
R1406	E-4
R1407	E-4
R1408	E-4
R1409	E-4
R1411	E-4
R1412	E-4
R1414	E-4
R1416	E-4
R1417	E-4
R1418	E-4
R1419	E-3
R1421	E-4
R1422	E-4
R1423	E-4
R1424	G-3
R1425	F-3
R1426	F-3
R1427	F-2
R1428	F-3
R1429	F-3
R1431	F-3
R1432	G-3
R1433	G-3
R1434	G-2
R1436	F-2
R1437	F-3
R1438	G-3
R1439	G-3
R1440	On R4
R1441	G-2
R1442	F-3
R1443	G-3
R1444	G-2
R1445	On R4
R1446	G-2
R1447	G-3
R1448	F-3
R1450	On R4
R1501	E-3
R1502	F-3
R1503	E-4
R1506	F-4
R1507	F-4
R1508	F-4
R1509	F-4
R1511	F-4
R1512	F-4
R1513	F-4
R1514	F-4
R1516	F-4
R1517	F-4
R1518	F-4
R1519	F-4
R1521	F-4
R1522	F-4
R1523	F-4
R1524	F-4
R1525	F-4
R1526	F-4
R1527	F-4
R1528	F-4
R1529	F-4
R1531	F-4
R1532	G-4
R1533	F-4
R1534	F-4
R1535	On tube
R1536	On tube
R1537	G-4
R1538	Power supply
R1539	Power supply
R1541	Power supply
R1542	Power supply
R1543	Power supply
R1544	Power supply
R1546	Power supply
R1547	Power supply
R1548	Power supply
R1549	Power supply
R1551	Power supply
R1552	F-3/F-4
R1553	F-3
R1554	F-3/F-4
R1601	B-2
R1602	B-2
R1603	B-2
R1604	B-2
R1606	B-2
R1607	B-2
R1608	B-2
R1609	B-2
R1611	B-2
R1612	B-2
R1613	B-2
R1614	B-2
R1616	B-2
R1617	B-2
R1618	A-2
R1619	A-2
V1	Tube
V201	Power supply
V202	Power supply
V203	Power supply
V204	Power supply
V206	Power supply
V207	Power supply
V208	Power supply
V209	Power supply
V211	Power supply
V212	Power supply
V213	Power supply
V214	Power supply
V216	Power supply
V217	Power supply
V218	Power supply
V219	Power supply
V221	Power supply
V222	Power supply
V223	Power supply
V224	Power supply
V226	High tension unit
V227	
V228	
V229	
V231	
V232	Power supply
V233	Power supply
V234	Power supply
V236	Power supply
V237	Power supply
V238	Power supply
V239	Power supply
V241	Power supply
V242	Power supply
V243	Power supply
V244	Power supply
V246	Power supply
V247	Power supply
V351	Att. unit
V352	Att. unit
V353	Att. unit
V354	Att. unit
V501	C-2
V504	B-2/C-2
V506	D-2
V507	D-2
V508	D-2/E-2
V509	D-2/E-2
V511	D-2
V512	D-2
V513	E-2
V514	E-2
V518	E-2
V519	E-2
V521	E-2
V522	E-2
V523	E-2
V524	E-2
V526	E-2
V601	C-3
V604	B-3/C-3
V606	D-3
V607	D-3
V608	D-3
V609	D-3
V611	D-2/D-3
V612	D-3
V613	D-3/E-3
V614	E-3
V616	E-3
V617	E-3
V618	E-3
V619	E-3
V621	E-3
V622	E-3
V623	E-3
V624	E-3
V626	E-3
V701	E-2
V702	E-2
V703	E-2
V704	E-2
V801	E-2
V802	F-3
V803	F-2
V804	F-2
V806	F-2
V807	F-2
V808	F-2
V809	E-2
V1001	C-3/C-4
V1002	C-4
V1003	B-4
V1004	B-4
V1006	B-3/C-3
V1008	B-4/C-4
V1009	B-4
V1011	B-4
V1012	B-4
V1013	C-4
V1014	C-4
V1016	C-4
V1017	B-4
V1201	D-3
V1202	D-4
V1203	D-4
V1204	D-4
V1206	D-4
V1207	D-4
V1208	D-4
V1209	D-4
V1211	D-4
V1212	D-4
V1213	D-4
V1214	D-4/E-4
V1216	D-3
V1217	D-3/E-3
V1218	E-4
V1219	D-4
V1221	D-4
V1222	D-3/D-4
V1223	E-3
V1401	E-4
V1402	E-4
V1403	E-4
V1404	E-4
V1406	E-4
V1407	E-4
V1408	E-4
V1409	E-4
V1411	E-4
V1412	F-2
V1413	F-2
V1414	F-2
V1416	F-3/G-3
V1417	F-3
V1419	G-3
V1421	G-3
V1422	G-2
V1423	G-2
V1424	G-2
V1426	G-2
V1427	G-2
V1428	G-2
V1501	D-4
V1502	E-4
V1503	E-4
V1504	F-4
V1506	F-3
V1508	E-4
V1511	F-4
V1512	F-4
V1513	F-4
V1514	F-4
V1516	F-4
V1517	F-4
V1518	F-4
V1519	G-4
V1521	B-2
V1522	B-2
V1601	B-2
V1602	B-2
V1603	B-2
V1604	B-2
D501	C-2
D601	C-3
D801	F-2/F-3
D802	Delay line
D1001	B-4
D1201	C-4/D-4
D1202	C-4/D-4
D1203	C-4/D-4
B1	LED
F201	Power supply
K501	C-2
K601	C-3
K1401	E-3
L201	Power supply
L202	Power supply
L203	Power supply
L801	F-2
L802	F-2
L1501	Trace rot. coil
T101	Rear panel
T201	Power supply
T202	Power supply

NOTES:


A
B
C
D
1
2
3
4
5
L1501
AQUADAG C.R.T.
A INPUT (from A attenuator switch S6 IIIR 18)
B INPUT (from B attenuator switch S8 III R18)
TO K501 (from S6 III F 8)
TO K601 (from S8 III F 8)
B AMPL./DIV.(R8)
A AMPL./DIV.(R7)
EXT. Z MOD.
R357 (trigger selector)
R362 (trigger selector)
12
X1 CAL.
A
S1A
ALT
S1B
CHOP
S1C
ADD
S1D
B
S1E
AUTO
S2A
AC
S2B
DC
S2C
TV
S2D
SLOPE
S3
K501
D501
K601
D601
D1001
D1201
D1202
D1203
3
4
5
S16a PT.5
INTENS (R1) POWER ON LAMP (B1)
INTENS (R1) WIPER
TRACE ROTATION (R10) WIPER
POWER ON LAMP (B1)
-12V
INTENS (R1) - TRACE ROTATION (R10)
+12V
-12D'
+12F'
LEVEL (R5)
WIPER
S10 IIIR POINTS 12 and 16
S10 IR 17 IF 17
TIME/DIV.(R9) CAL.(S11)
WIPER
S10 IIIR 14 IIF 17
TIME/DIV (R9) CAL.(S11)
+12H
S10 IIF 20 IIF 19

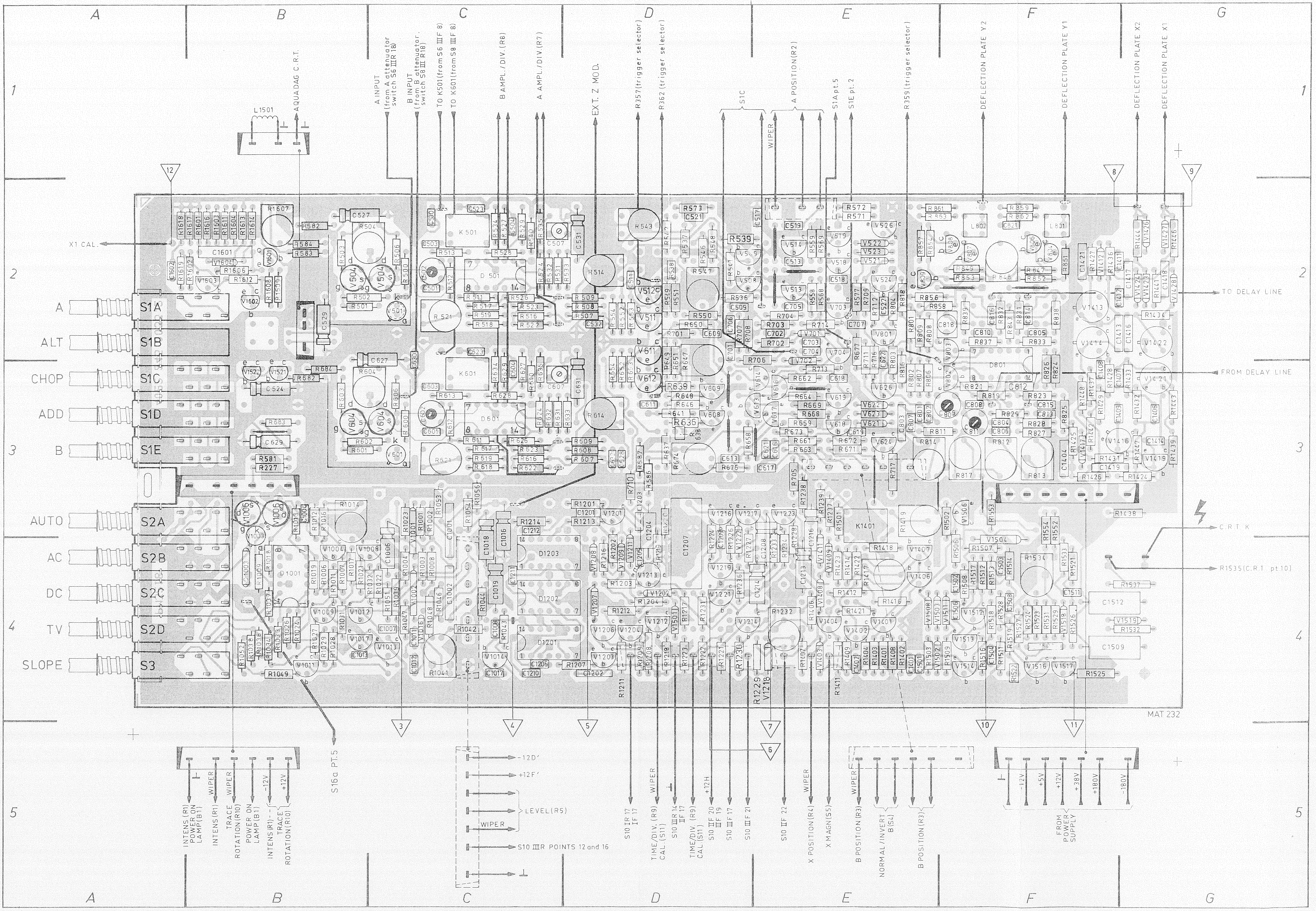

A
B
C
D
E
F
G
1
2
3
4
5
L1501
AQUADAG C.R.T.
A INPUT (from A attenuator switch S6 IIIR 18)
B INPUT (from B attenuator switch S8 IIIR 18)
TO K501 (from S6 IIIF 8)
TO K601 (from S8 IIIF 8)
B AMPL./DIV. (R8)
A AMPL./DIV. (R7)
EXT. Z MOD.
R357 (trigger selector)
R362 (trigger selector)
S1C
WIPER
A POSITION (R2)
S1A pt.5
S1E pt.2
R359 (trigger selector)
DEFLECTION PLATE Y2
DEFLECTION PLATE Y1
DEFLECTION PLATE X2
DEFLECTION PLATE X1
X1 CAL.
TO DELAY LINE
FROM DELAY LINE
C.R.T. K
R1535 (C.R.T. pt.10)
A
ALT
CHOP
ADD
B
AUTO
AC
DC
TV
SLOPE
S1A
S1B
S1C
S1D
S1E
S2A
S2B
S2C
S2D
S3
MAT 232
S16a PT.5
INTENS (R1) POWER ON LAMP (B1)
INTENS (R1)
WIPER
TRACE ROTATION (R10)
WIPER
POWER ON LAMP (B1)
INTENS (R1) - TRACE ROTATION (R10)
-12V
+12V
+12D'
+12F'
LEVEL (R5)
WIPER
S10 IIIR POINTS 12 and 16
S10 IR 17 IF 17
TIME/DIV. (R9) CAL (S11)
WIPER
S10 IIIR 14 IIF 17
TIME/DIV. (R9) CAL (S11)
+12H
S10 IIF 20 IIIF 19
S10 IIF 17
S10 IIF 21
S10 IIF 22
X POSITION (R4)
WIPER
X MAGN (S5)
WIPER
B POSITION (R3)
NORMAL/INVERT B (S4)
B POSITION (R3)
-12V
+5V
+12V
+38V
+180V
-180V
FROM POWER SUPPLY
3
4
5
6
7
8
9
10
11
12

Fig. 3.49. Amplifier p.c. board with rear side tracks

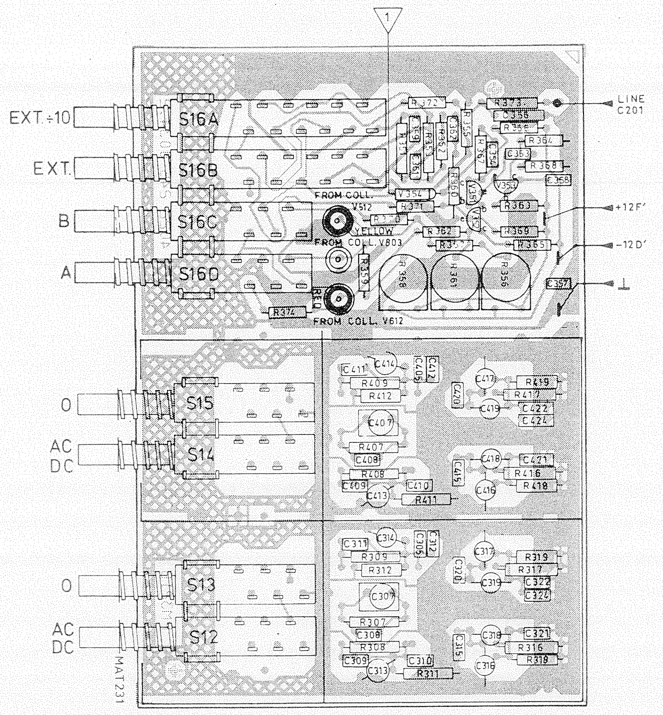

EXT.÷10
EXT.
B
A
S16A
S16B
S16C
S16D
LINE C201
+12F'
-12D'
FROM COLL. V803
FROM COLL. V612
YELLOW
0
AC
DC
S15
S14
S13
S12
MAT 231

Fig. 3.50. Vertical attenuator p.c. board

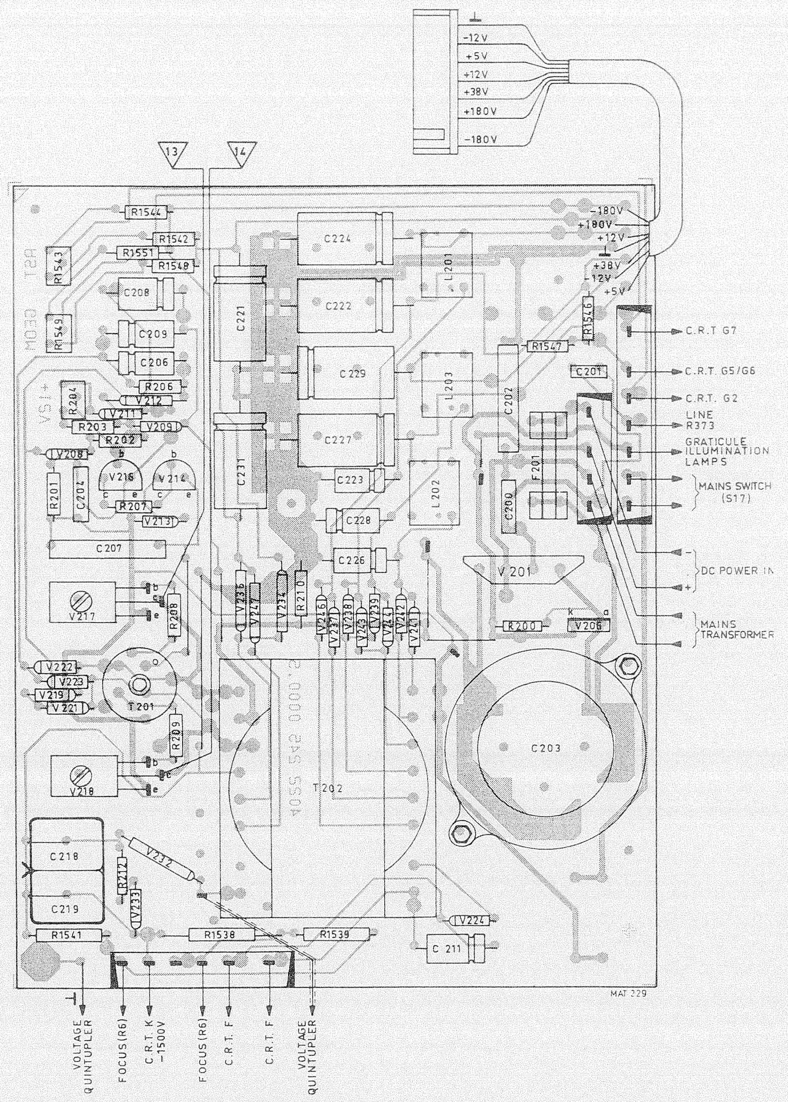
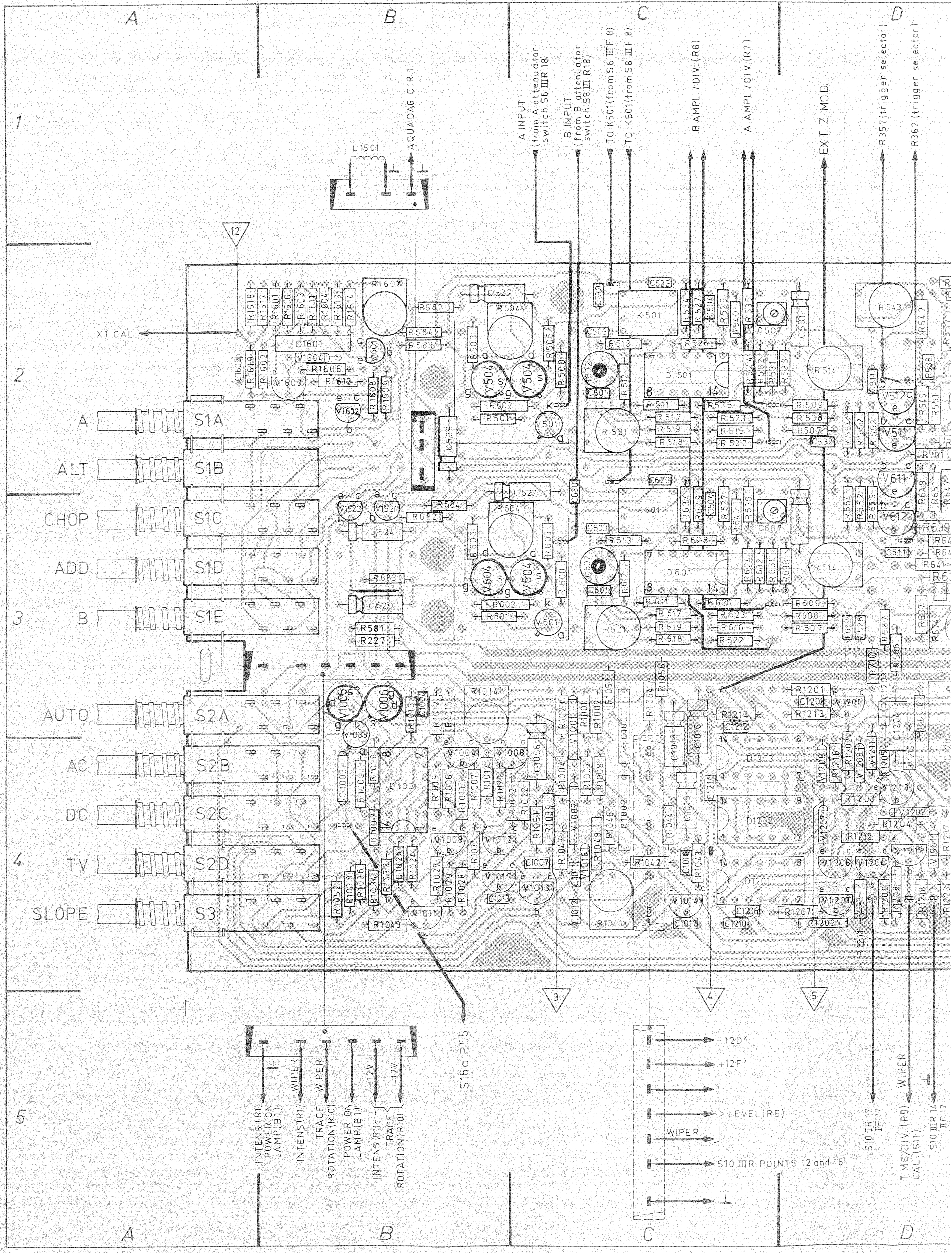

-12V
+5V
+12V
+38V
+180V
-180V
13
14
C.R.T. G7
C.R.T. G5/G6
C.R.T. G2
LINE R373
GRATICULE ILLUMINATION LAMPS
MAINS SWITCH (S17)
DC POWER IN
MAINS TRANSFORMER
VOLTAGE QUINTUPLER
FOCUS (R6)
C.R.T. K -1500V
FOCUS (R6)
C.R.T. F
C.R.T. F
VOLTAGE QUINTUPLER
MAT 229

Fig. 3.51. Power supply p.c. board


A
B
C
D
1
2
3
4
5
AQUADAG C.R.T.
L1501
A INPUT (from A attenuator switch S6 IIIR 18)
B INPUT (from B attenuator switch S8 III R18)
TO K501 (from S6 III F 8)
TO K601 (from S8 III F 8)
B AMPL./DIV. (R8)
A AMPL./DIV. (R7)
EXT. Z MOD.
R357 (trigger selector)
R362 (trigger selector)
12
X1 CAL.
A
ALT
CHOP
ADD
B
S1A
S1B
S1C
S1D
S1E
AUTO
AC
DC
TV
SLOPE
S2A
S2B
S2C
S2D
S3
3
4
5
S16a PT.5
INTENS (R1) POWER ON LAMP (B1)
INTENS (R1)
WIPER
TRACE ROTATION (R10)
WIPER
POWER ON LAMP (B1)
INTENS (R1)
TRACE ROTATION (R10)
-12V
+12V
-12D'
+12F'
LEVEL (R5)
WIPER
S10 IIIR POINTS 12 and 16
S10 IR 17 IF 17
TIME/DIV. (R9) CAL. (S11)
WIPER
S10 IIIR 14 IIF 17

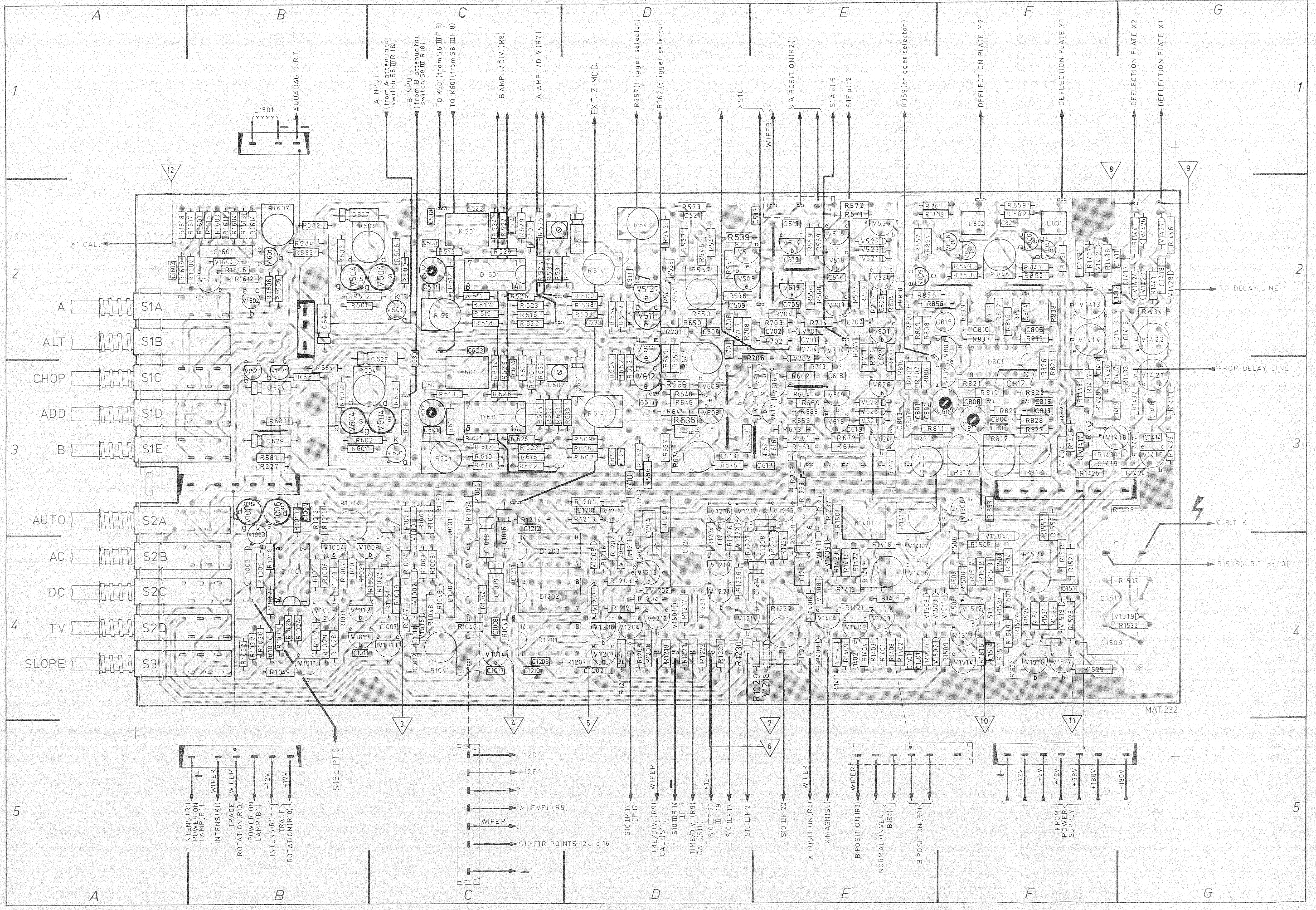
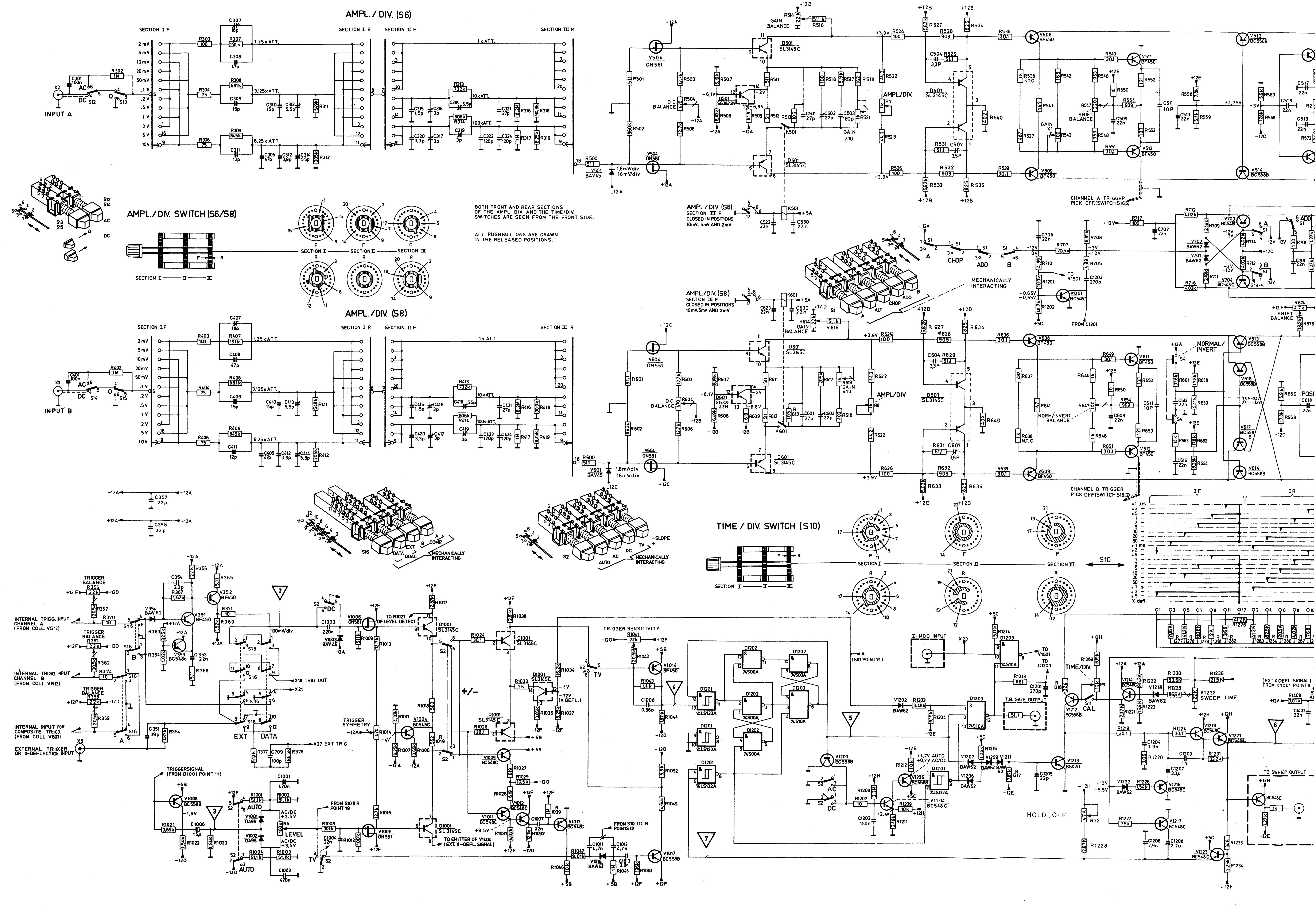

A
B
C
D
E
F
G
1
2
3
4
5
L1501
AQUADAG C.R.T.
A INPUT (from A attenuator switch S6 III R 18)
B INPUT (from B attenuator switch S8 III R 18)
TO K501 (from S6 III F 8)
TO K601 (from S8 III F 8)
B AMPL./DIV. (R8)
A AMPL./DIV. (R7)
EXT. Z MOD.
R357 (trigger selector)
R362 (trigger selector)
S1C
WIPER
A POSITION (R2)
S1A pt.5
S1E pt.2
R359 (trigger selector)
DEFLECTION PLATE Y2
DEFLECTION PLATE Y1
DEFLECTION PLATE X2
DEFLECTION PLATE X1
X1 CAL.
TO DELAY LINE
FROM DELAY LINE
C.R.T. K
R1535 (C.R.T. pt.10)
A
ALT
CHOP
ADD
B
S1A
S1B
S1C
S1D
S1E
AUTO
AC
DC
TV
SLOPE
S2A
S2B
S2C
S2D
S3
MAT 232
S16a PT.5
INTENS (R1) POWER ON LAMP (B1)
WIPER
INTENS (R1)
WIPER
TRACE ROTATION (R10)
POWER ON LAMP (B1)
-12V
INTENS (R1) -- TRACE ROTATION (R10)
+12V
-12D'
+12F'
LEVEL (R5)
WIPER
S10 III R POINTS 12 and 16
S10 I R 17 I F 17
WIPER
TIME/DIV. (R9) CAL. (S11)
S10 III R 14 II F 17
TIME/DIV. (R9) CAL. (S11)
+12H
S10 III F 20 III F 19
S10 III F 17
S10 III F 21
S10 II F 22
WIPER
X POSITION (R4)
X MAGN. (S5)
WIPER
B POSITION (R3)
NORMAL/INVERT B (S4)
B POSITION (R3)
-12V
+5V
+12V
+38V
+180V
-180V
FROM POWER SUPPLY
3
4
5
6
7
8
9
10
11
12

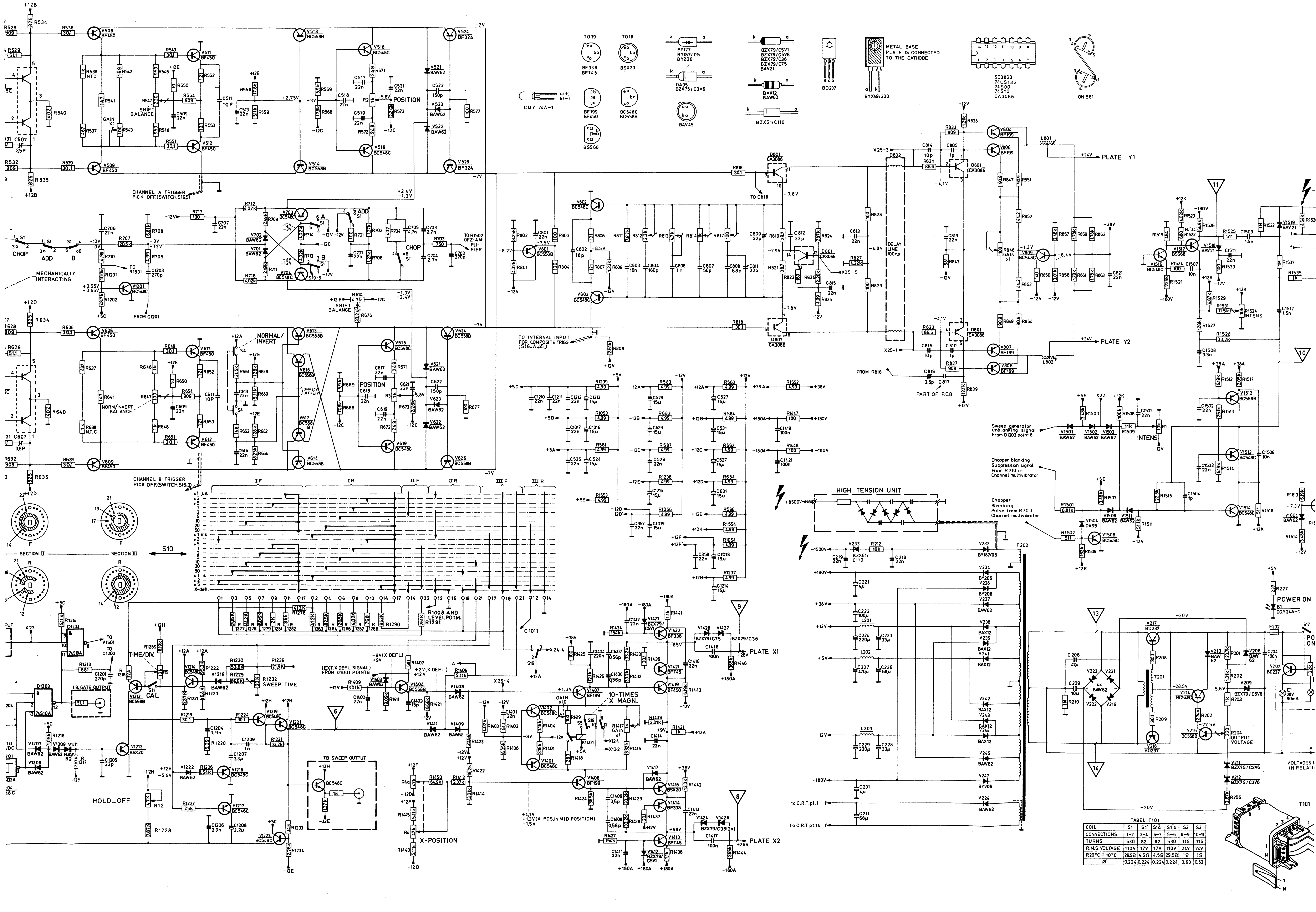
Fig. 3.52. Amplifier p.c. board with upper side tracks



BOTH FRONT AND REAR SECTIONS OF THE AMPL. DIV. AND THE TIME/DIV. SWITCHES ARE SEEN FROM THE FRONT SIDE.

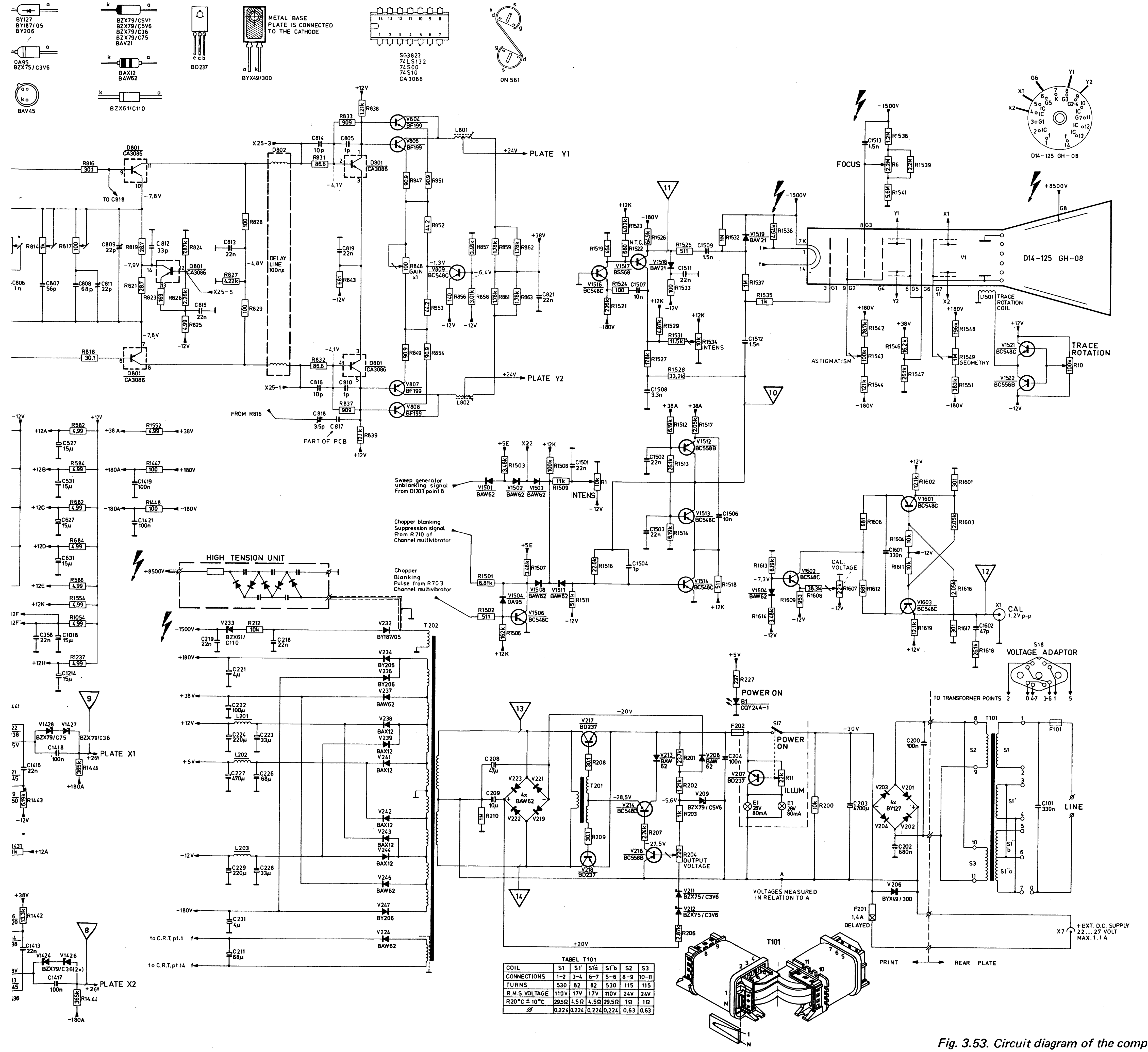
ALL PUSHBUTTONS ARE DRAWN IN THE RELEASED POSITIONS.

AMPL./DIV. (S6)
SECTION I F
SECTION I R
SECTION II F
SECTION III R
2 mV
5 mV
10 mV
20 mV
50 mV
.1 V
.2 V
.5 V
1 V
2 V
5 V
10 V
1,25 x ATT.
3,125 x ATT.
6,25 x ATT.
1 x ATT.
10 x ATT.
100 x ATT.
INPUT A
INPUT B
AC
DC
S12
S13
S14
S15
AMPL./DIV. SWITCH (S6/S8)
SECTION I — II — III
AMPL./DIV. (S8)
V504
ON561
V501
BAV45
1,6 mV/div
16 mV/div
D501
SL3145C
D.C. BALANCE
GAIN BALANCE
GAIN X10
AMPL./DIV.
K501
AMPL./DIV. (S6) SECTION III F CLOSED IN POSITIONS 10mV, 5mV AND 2mV
AMPL./DIV. (S8) SECTION III F CLOSED IN POSITIONS 10mV, 5mV AND 2mV
V508 BF450
V509 BF450
V511 BF450
V512 BF450
V513 BC558B
V514 BC558B
SHIFT BALANCE
GAIN X1
CHANNEL A TRIGGER PICK OFF (SWITCH S16,5)
CHANNEL B TRIGGER PICK OFF (SWITCH S16,2)
CHOP
ADD
ALT
A
B
MECHANICALLY INTERACTING
V1201 BC548C
FROM C1201
TO R1501
V601 BAV45
V604 ON561
D601 SL3145C
K601
V608 BF450
V609 BF450
V611 BF450
V612 BF450
V613 BC558B
V614 BC558B
V616 BC558B
V617 BC558B
NORMAL/INVERT
NORM/INVERT BALANCE
SHIFT BALANCE
V702 BAW62
V701 BAW62
V703 BC548C
V704 BC548C
TIME / DIV. SWITCH (S10)
SECTION I
SECTION II
SECTION III
S10
X-defl.
S16
DATA
EXT
QUAL
COMP.
MECHANICALLY INTERACTING
S2
AUTO
AC
DC
TV
SLOPE
TRIGGER BALANCE
INTERNAL TRIGG. INPUT CHANNEL A (FROM COLL. V512)
INTERNAL TRIGG. INPUT CHANNEL B (FROM COLL. V612)
INTERNAL INPUT FOR COMPOSITE TRIGG. (FROM COLL. V803)
EXTERNAL TRIGGER OR X-DEFLECTION INPUT
X5
V354 BAW62
V351 BF450
V352 BF450
V353 BC548C
X18 TRIG OUT
X21
X27 EXT TRIG
TRIGGERSIGNAL (FROM D1001 POINT 11)
V1008 BC558B
V1001 OA95
V1002 OA95
AUTO
AC/DC +3,5V
AC/DC -3,5V
LEVEL
FROM S10 II R POINT 19
V1006 ON561
V1003 BAV45
TO R1021 OF LEVEL DETECT.
D1001 SL3145C
TRIGGER SYMMETRY
V1004 BC548C
V1009 BC548C
V1011 BC548C
V1012 BC548C
V1013 BC548C
V1016 BAW62
V1017 BC558B
V1014 BF450
+/-
TO EMITTER OF V1404 (EXT. X-DEFL. SIGNAL)
FROM S10 III R POINTS 12
TRIGGER SENSITIVITY
(X DEFL.)
D1201 74LS132A
D1202 74S00A
D1203 74S10A
A (S10 POINT 21)
Z-MOD INPUT
X23
TO V1501
TO C1203
T.B. GATE OUTPUT
V1202 BAW62
V1203 BC558B
V1206 BC558B
V1204 BC548C
V1207 BAW62
V1208 BAW62
V1209 BAW62
V1211 BAW62
+4,7V AUTO +0,7V AC/DC
V1213 BSX20
HOLD_OFF
TIME/DIV. CAL
V1212 BC558B
S11
V1214 BC548C
V1218 BAW62
SWEEP TIME
(EXT. X DEFL. SIGNAL) FROM D1001 POINTS
V1219 BC548C
V1221 BC548C
V1222 BAW62
V1216 BC548C
V1217 BC548C
V1223 BC548C
TB SWEEP OUTPUT


CHANNEL A TRIGGER PICK OFF.(SWITCH.S16,5)
CHANNEL B TRIGGER PICK OFF.(SWITCH.S16,2)
SHIFT BALANCE
GAIN X1
POSITION
CHOP
ADD
MECHANICALLY INTERACTING
NORMAL/ INVERT
NORM/INVERT BALANCE
TO R1502 OFZ-AMPLIFIER
TO INTERNAL INPUT FOR COMPOSITE TRIGG (S16-A.p5.)
DELAY LINE 100ns
PLATE Y1
PLATE Y2
FROM R816
PART OF P.C.B
INTENS
Sweep generator unblanking signal From D1203 point 8
Chopper blanking Suppression signal From R 710 of Channel multivibrator
Chopper Blanking Pulse from R 703 Channel multivibrator
HIGH TENSION UNIT
+8500V
-1500V
T202
to C.R.T. pt.1
to C.R.T. pt.14
POWER ON
VOLTAGES IN RELATION
OUTPUT VOLTAGE
T201
T101
SECTION II
SECTION III
S10
TIME/DIV.
CAL
SWEEP TIME
HOLD_OFF
T.B. GATE OUTPUT
TB SWEEP OUTPUT
X-POSITION
(EXT.X DEFL.SIGNAL) FROM D1001 POINT8
10-TIMES X MAGN.
GAIN x10
GAIN x1
PLATE X1
PLATE X2
+4,1V +1,3V (X-POS.in MID POSITION) -1,5V
R1008 AND LEVELPOTM.
I F
I R
II F
II R
III F
III R
X-defl.
METAL BASE PLATE IS CONNECTED TO THE CATHODE
BYX49/300
BD237
SG3823 74LS132 74S00 74S10 CA3086
ON 561
COY 24A-1
TO39 BF338 BF745
TO18 BSX20
BF199 BF450
BC548C BC558B
BSS68
BAV45
BY127 BY187/05 BY206
OA95 BZX75/C3V6
BZX79/C5V1 BZX79/C5V6 BZX79/C36 BZX79/C75 BAV21
BAX12 BAW62
BZX61/C110

TABEL T101

COIL	S1	S1′	S1″a	S1″b	S2	S3
CONNECTIONS	1–2	3–4	6–7	5–6	8–9	10–11
TURNS	530	82	82	530	115	115
R.M.S. VOLTAGE	110V	17V	17V	110V	24V	24V
R20°C ± 10°C	29,5Ω	4,5 Ω	4,5Ω	29,5Ω	1Ω	1Ω
Ø	0,224	0,224	0,224	0,224	0,63	0,63


BY127
BY187/05
BY206
OA95
BZX75/C3V6
BAV45
BZX79/C5V1
BZX79/C5V6
BZX79/C36
BZX79/C75
BAV21
BAX12
BAW62
BZX61/C110
BD237
METAL BASE PLATE IS CONNECTED TO THE CATHODE
BYX49/300
SG3823
74LS132
74S00
74S10
CA3086
ON 561
D14-125 GH-08
PLATE Y1
PLATE Y2
DELAY LINE 100ns
FOCUS
ASTIGMATISM
GEOMETRY
TRACE ROTATION
TRACE ROTATION COIL
INTENS
GAIN x1
HIGH TENSION UNIT
Sweep generator unblanking signal From D1203 point 8
Chopper blanking Suppression signal From R710 of Channel multivibrator
Chopper Blanking Pulse from R703 Channel multivibrator
CAL VOLTAGE
CAL 1,2V p-p
S18 VOLTAGE ADAPTOR
POWER ON
ILLUM
OUTPUT VOLTAGE
VOLTAGES MEASURED IN RELATION TO A
TO TRANSFORMER POINTS
LINE
+EXT. D.C. SUPPLY 22...27 VOLT MAX. 1,1 A
F201 1,4A DELAYED
PRINT
REAR PLATE
PLATE X1
PLATE X2
to C.R.T. pt.1
to C.R.T. pt.14
FROM R816
PART OF P.CB
+8500V
-1500V

TABEL T101

COIL	S1	S1′	S1″a	S1″b	S2	S3
CONNECTIONS	1–2	3–4	6–7	5–6	8–9	10–11
TURNS	530	82	82	530	115	115
R.M.S. VOLTAGE	110V	17V	17V	110V	24V	24V
R20°C ± 10°C	29,5Ω	4,5Ω	4,5Ω	29,5Ω	1Ω	1Ω
⌀	0,224	0,224	0,224	0,224	0,63	0,63

- FOR THE SETTINGS OF THE OSCILLOSCOPE UNDER TEST SEE CHAPTER 3,4,2.
- FOR MEASURING THESE WAVE-FORMS A PROBE 10:1 MUST BE USED.
- HOLD-OFF CONTROL FULLY CLOCKWISE

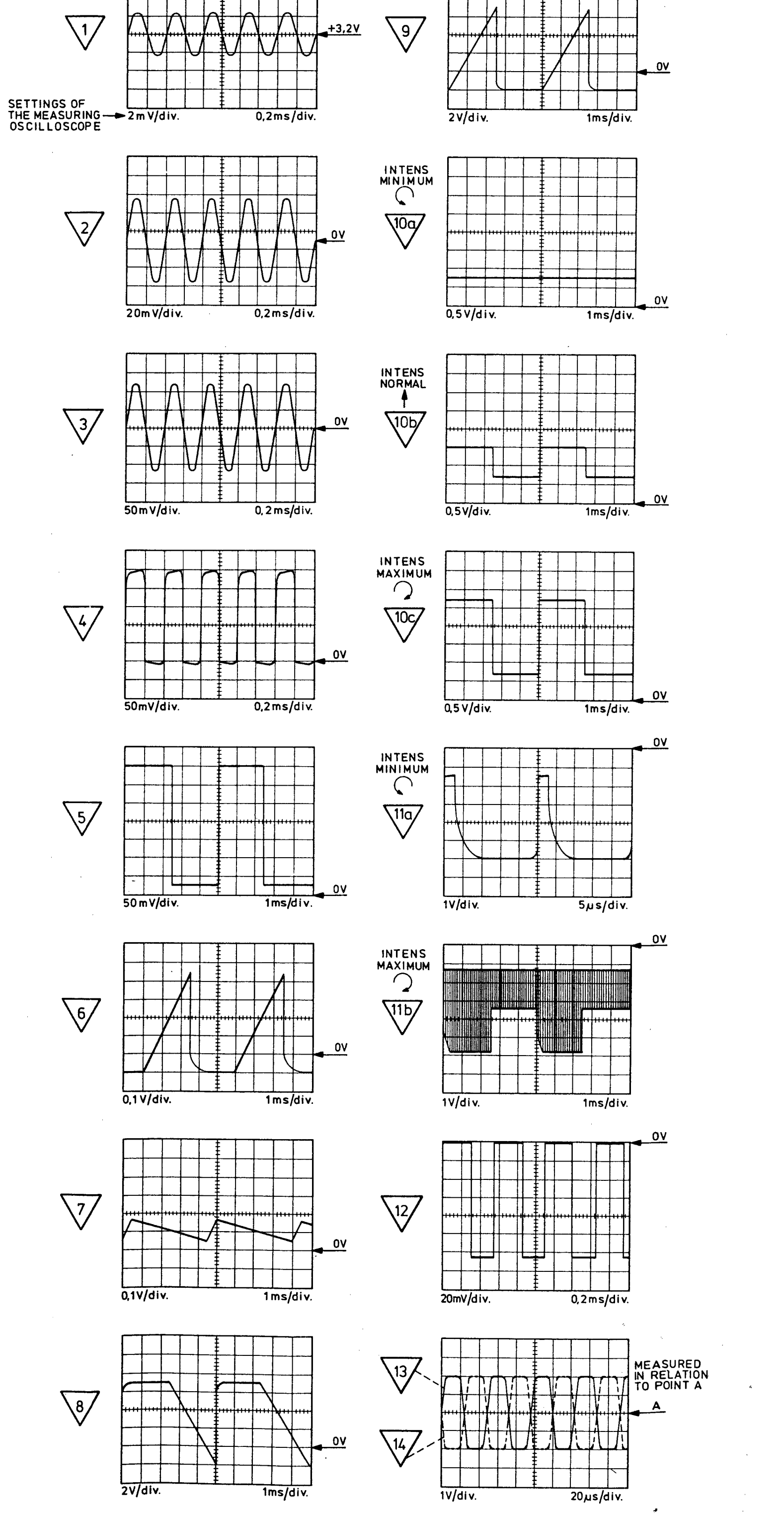


Fig. 3.53. Circuit diagram of the complete oscilloscope part

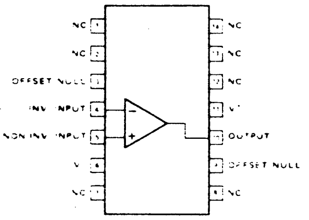
3.10. TRUTH TABLES & PIN CONFIGURATIONS OF I.C.'S USED

HIGH SPEED DUAL DIFFERENTIAL COMPARATOR/SENSE AMP NE521

D-2001

PIN CONFIGURATIONS

F,N-14 PACKAGE

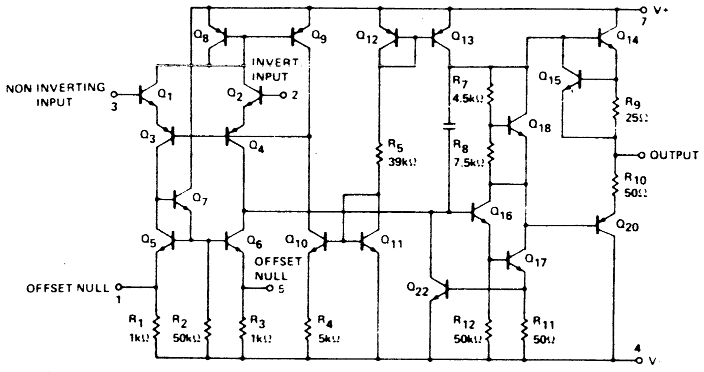

NC 1
NC 2
OFFSET NULL 3
INV INPUT 4
NON INV INPUT 5
V 6
NC 7
14 NC
13 NC
12 NC
11 V+
10 OUTPUT
9 OFFSET NULL
8 NC
−
+

ORDER PART NO.

μA741F
μA741N-14
μA741CF
μA741CN-14
SA741CF
SA741CN-14

EQUIVALENT SCHEMATIC

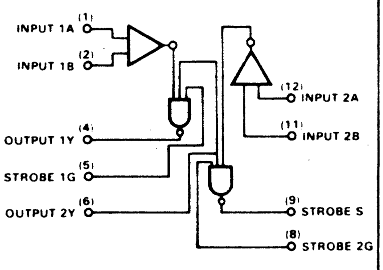
μA741, A741C, SA741C
ONE AMPLIFIER OF MC1558, MC1458, SA1458


V+
7
Q8
Q9
Q12
Q13
Q14
INVERT INPUT
NON INVERTING INPUT 3
Q1
Q2
2
R7 4.5kΩ
Q15
R9 25Ω
Q3
Q4
R5 39kΩ
R8 7.5kΩ
Q18
OUTPUT
R10 50Ω
Q7
Q16
Q20
Q5
Q6
Q10
Q11
OFFSET NULL 5
Q17
OFFSET NULL 1
Q22
R1 1kΩ
R2 50kΩ
R3 1kΩ
R4 5kΩ
R12 50kΩ
R11 50Ω
4
V

GENERAL PURPOSE OPERATIONAL AMPLIFIER μA741CN

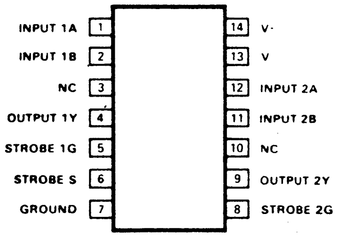
D-2002

BLOCK DIAGRAM


(1) INPUT 1A
(2) INPUT 1B
(4) OUTPUT 1Y
(5) STROBE 1G
(6) OUTPUT 2Y
(12) INPUT 2A
(11) INPUT 2B
(9) STROBE S
(8) STROBE 2G

PIN CONFIGURATION

F,N PACKAGE


INPUT 1A 1
INPUT 1B 2
NC 3
OUTPUT 1Y 4
STROBE 1G 5
STROBE S 6
GROUND 7
14 V+
13 V
12 INPUT 2A
11 INPUT 2B
10 NC
9 OUTPUT 2Y
8 STROBE 2G

OCTAL BUFFERS (3-STATE) 74 SERIES "244"

D-2003
D-2004

D-2006
D-2007

PIN CONFIGURATION

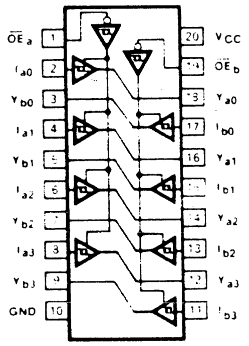

$\overline{OE}_a$
I_{a0}
Y_{b0}
I_{a1}
Y_{b1}
I_{a2}
Y_{b2}
I_{a3}
Y_{b3}
GND
1
2
3
4
5
6
7
8
9
10
20
19
18
17
16
15
14
13
12
11
V_{CC}
$\overline{OE}_b$
Y_{a0}
I_{b0}
Y_{a1}
I_{b1}
Y_{a2}
I_{b2}
Y_{a3}
I_{b3}

Figure A

TRUTH TABLE

INPUTS				OUTPUTS	
$\overline{OE}_a$	I_a	$\overline{OE}_b$	I_b	Y_a	Y_b
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	(Z)	(Z)

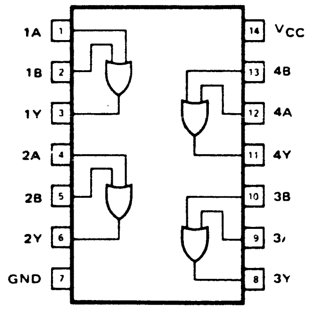
H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance (off) state

QUAD 2-INPUT OR GATE 7432

D-2008
D-2069

PIN CONFIGURATION

A,F,W PACKAGE


1A
1B
1Y
2A
2B
2Y
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
V_{CC}
4B
4A
4Y
3B
3A
3Y

Positive logic: y = A+B

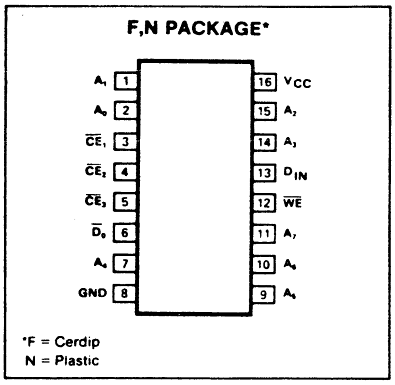
TRUTH TABLE

A	B	X
0	0	0
1	0	1
0	1	1
1	1	1

256 BIT BIPOLAR RAM (256X1) 82S117 (O.C.)

D-2009
D-2011

PIN CONFIGURATION


F,N PACKAGE*
A_1 1
A_0 2
$\overline{CE}_1$ 3
$\overline{CE}_2$ 4
$\overline{CE}_3$ 5
$\overline{D}_0$ 6
A_4 7
GND 8
16 V_{CC}
15 A_2
14 A_3
13 D_{IN}
12 $\overline{WE}$
11 A_7
10 A_6
9 A_5

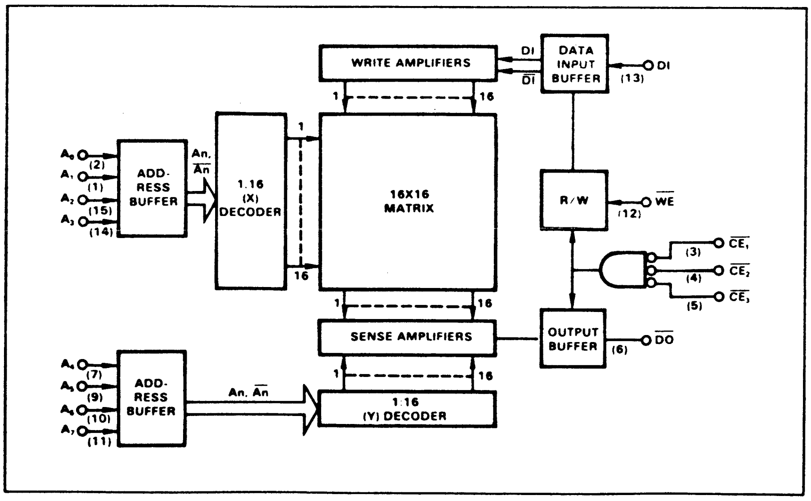
*F = Cerdip
N = Plastic

TRUTH TABLE

MODE	$\overline{CE}$*	$\overline{WE}$	D_{IN}	$\overline{D}_{OUT}$	
				82S16/116	82S17/117
Read	0	1	X	Stored $\overline{\text{data}}$	Stored $\overline{\text{data}}$
Write "0"	0	0	0	1	1
Write "1"	0	0	1	0	0
Diasabled	1	X	X	High-Z	1

*"0" = All $\overline{CE}$ inputs low; "1" = one or more $\overline{CE}$ inputs high.
X = Don't care.

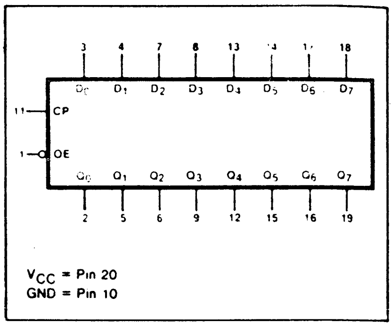
BLOCK DIAGRAM


WRITE AMPLIFIERS
DI
$\overline{DI}$
DATA INPUT BUFFER
(13)
DI
1
16
1
16
A_0 (2)
A_1 (1)
A_2 (15)
A_3 (14)
ADD-RESS BUFFER
An, $\overline{An}$
1.16 (X) DECODER
16X16 MATRIX
R/W
(12)
$\overline{WE}$
(3) $\overline{CE}_1$
(4) $\overline{CE}_2$
(5) $\overline{CE}_3$
1
16
SENSE AMPLIFIERS
OUTPUT BUFFER
(6)
$\overline{DO}$
1
16
A_4 (7)
A_5 (9)
A_6 (10)
A_7 (11)
ADD-RESS BUFFER
An, $\overline{An}$
1:16 (Y) DECODER

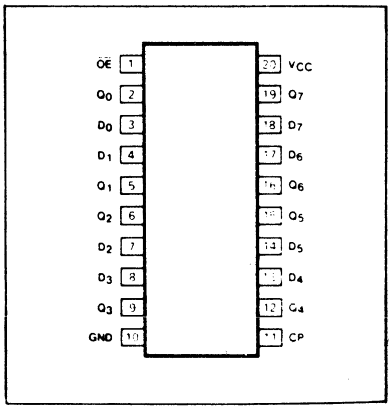
OCTAL D FLIP-FLOP WITH 3-STATE OUTPUTS — 74 SERIES "374"

D-2012
D-2013
D-2022

LOGIC SYMBOL


3 4 7 8 13 14 17 18
D0 D1 D2 D3 D4 D5 D6 D7
11 CP
1 OE
Q0 Q1 Q2 Q3 Q4 Q5 Q6 Q7
2 5 6 9 12 15 16 19
V_{CC} = Pin 20
GND = Pin 10

PIN CONFIGURATION

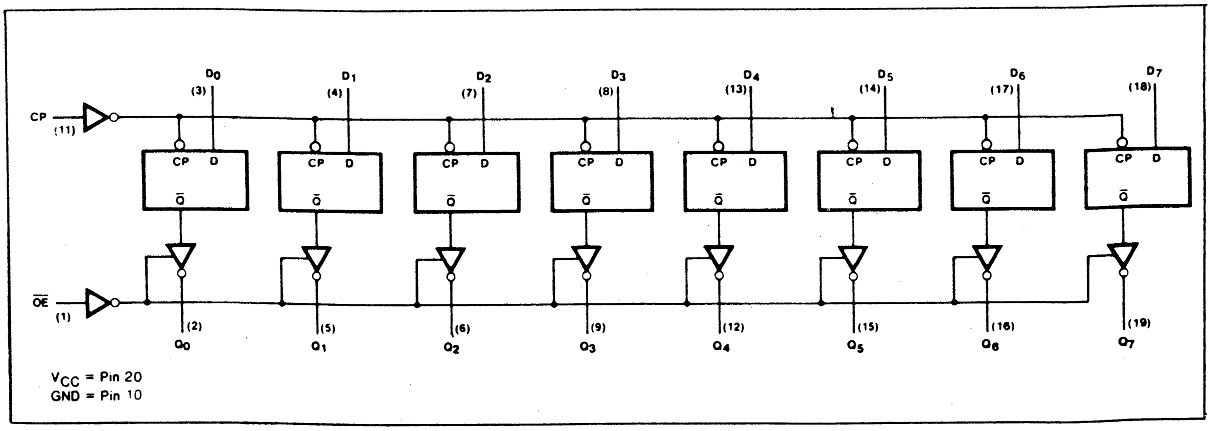

$\overline{OE}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 VCC
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 CP

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS			INTERNAL REGISTER	OUTPUTS
	$\overline{OE}$	CP	D_n		Q_0-Q_7
Load & read register	L L	↑ ↑	l h	L H	L H
Load register & disable outputs	H H	↑ ↑	l h	L H	(Z) (Z)

H = HIGH voltage level
h = HIGH voltage level one setup time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition
(Z) = HIGH impedance "off" state
↑ = LOW-to-HIGH clock transition

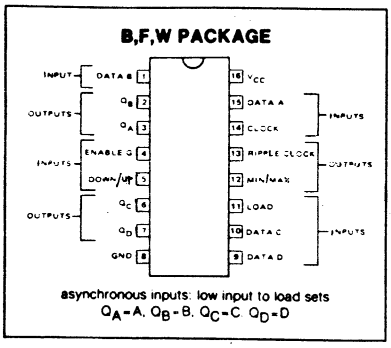
LOGIC DIAGRAM


D_0 (3)
D_1 (4)
D_2 (7)
D_3 (8)
D_4 (13)
D_5 (14)
D_6 (17)
D_7 (18)
CP (11)
CP D
$\bar{Q}$
$\overline{OE}$ (1)
(2) Q_0
(5) Q_1
(6) Q_2
(9) Q_3
(12) Q_4
(15) Q_5
(16) Q_6
(19) Q_7
V_{CC} = Pin 20
GND = Pin 10

SYNCHRONOUS BINARY UP/DOWN COUNTER 74191

D-2014
D-2017

PIN CONFIGURATION


B,F,W PACKAGE
INPUT
DATA B
1
OUTPUTS
Q_B
2
Q_A
3
INPUTS
ENABLE G
4
DOWN/UP
5
OUTPUTS
Q_C
6
Q_D
7
GND
8
16
V_{CC}
15
DATA A
14
CLOCK
INPUTS
13
RIPPLE CLOCK
12
MIN/MAX
OUTPUTS
11
LOAD
10
DATA C
9
DATA D
INPUTS

asynchronous inputs: low input to load sets
Q_A=A, Q_B=B, Q_C=C, Q_D=D

BLOCK DIAGRAM

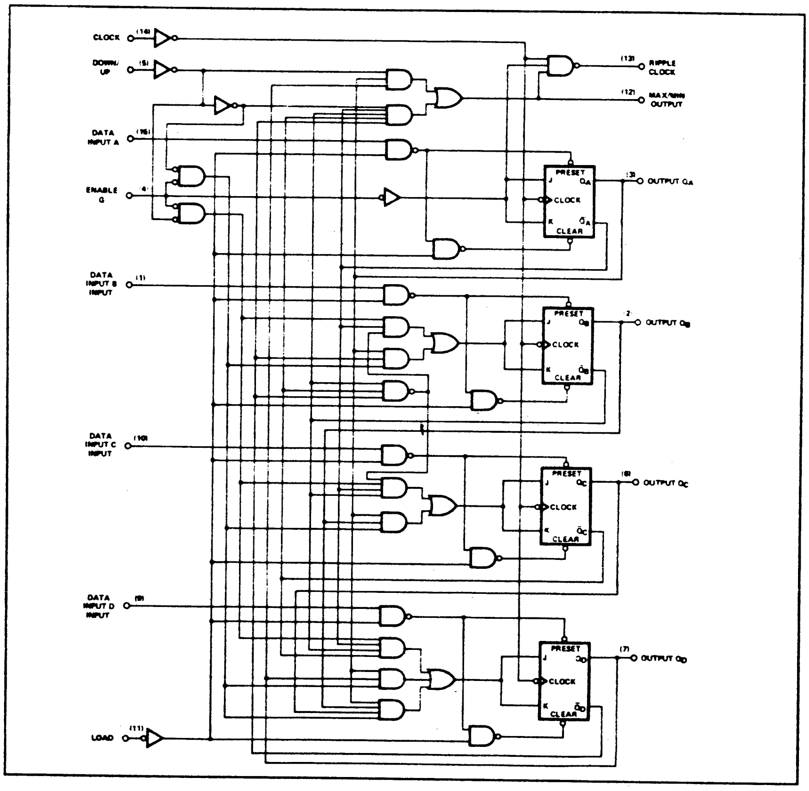
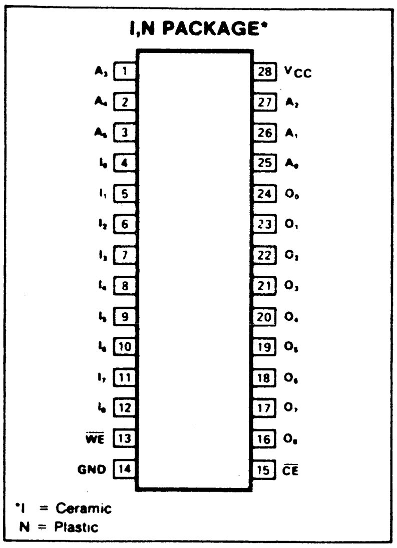

CLOCK
(14)
DOWN/UP
(5)
DATA INPUT A
(15)
ENABLE G
(4)
DATA INPUT B INPUT
(1)
DATA INPUT C INPUT
(10)
DATA INPUT D INPUT
(9)
LOAD
(11)
(13)
RIPPLE CLOCK
(12)
MAX/MIN OUTPUT
PRESET
J
Q_A
CLOCK
K
$\bar{Q}_A$
CLEAR
(3)
OUTPUT Q_A
PRESET
J
Q_B
CLOCK
K
$\bar{Q}_B$
CLEAR
(2)
OUTPUT Q_B
PRESET
J
Q_C
CLOCK
K
$\bar{Q}_C$
CLEAR
(6)
OUTPUT Q_C
PRESET
J
Q_D
CLOCK
K
$\bar{Q}_D$
CLEAR
(7)
OUTPUT Q_D

TABLE identical to: D2024
D2026
D2027
D2028

576-BIT BIPOLAR RAM (64X9) 82S09 (D.C.)

D-2018
D-2019

PIN CONFIGURATION


I,N PACKAGE*
A3 1
A4 2
A5 3
I0 4
I1 5
I2 6
I3 7
I4 8
I5 9
I6 10
I7 11
I8 12
WE 13
GND 14
28 VCC
27 A2
26 A1
25 A0
24 O0
23 O1
22 O2
21 O3
20 O4
19 O5
18 O6
17 O7
16 O8
15 CE

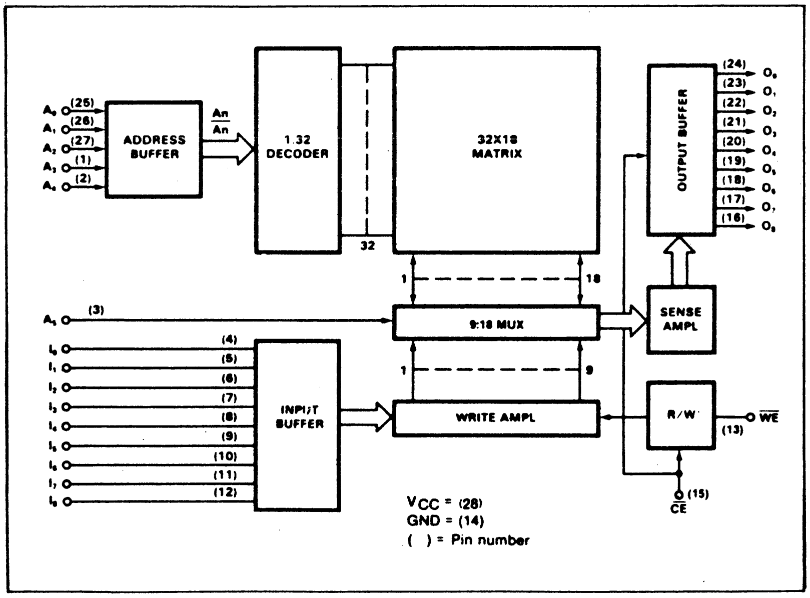
*I = Ceramic
N = Plastic

TRUTH TABLE

MODE	CE	WE	I_N	
Read	0	1	X	Complement of data stored
Write "0"	0	0	0	1
Write "1"	0	0	1	0
Disabled	1	X	X	1

X = Don't care

BLOCK DIAGRAM


A0 (25)
A1 (26)
A2 (27)
A3 (1)
A4 (2)
ADDRESS BUFFER
An
An
1:32 DECODER
32
32X18 MATRIX
1
18
A5 (3)
9:18 MUX
1
9
SENSE AMPL
OUTPUT BUFFER
(24) O0
(23) O1
(22) O2
(21) O3
(20) O4
(19) O5
(18) O6
(17) O7
(16) O8
I0 (4)
I1 (5)
I2 (6)
I3 (7)
I4 (8)
I5 (9)
I6 (10)
I7 (11)
I8 (12)
INPUT BUFFER
WRITE AMPL
R/W
WE (13)
(15) CE

VCC = (28)
GND = (14)
( ) = Pin number

QUAD 2-INPUT NAND GATE — 74 SERIES "00"

D-2021
D-2034
D-2052

PIN CONFIGURATIONS

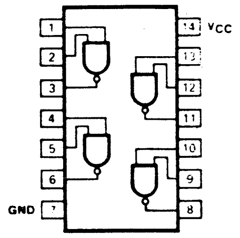

1
2
3
4
5
6
GND 7
14 VCC
13
12
11
10
9
8

Figure A

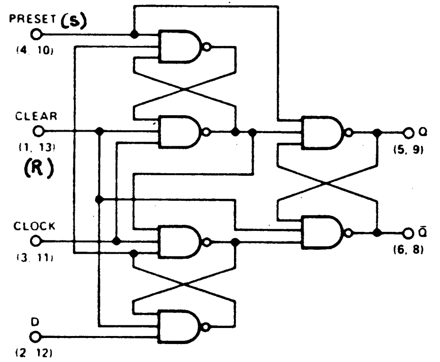
TRUTH TABLE

A	B	X
0	0	1
1	0	1
0	1	1
1	1	0

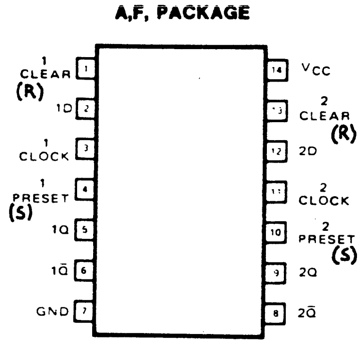
DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP — 7474

D-2023
D-2036
D-2052
D-2071

FUNCTIONAL BLOCK DIAGRAM (Each Flip-Flop)


PRESET (S)
(4, 10)
CLEAR
(1, 13)
(R)
CLOCK
(3, 11)
D
(2, 12)
Q
(5, 9)
Q̄
(6, 8)

PIN CONFIGURATION


A,F, PACKAGE
1 CLEAR (R) 1
1D 2
1 CLOCK 3
1 PRESET (S) 4
1Q 5
1Q̄ 6
GND 7
14 VCC
13 2 CLEAR (R)
12 2D
11 2 CLOCK
10 2 PRESET (S)
9 2Q
8 2Q̄

DESCRIPTION

Preset and clear inputs are active-low and operate independently of the clock input. When preset and clear are inactive (high), information at the D input is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level of the clock pulse and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D-input signal has no effect at the output.

TRUTH TABLE (Each Flip-Flop)

Inputs				Outputs	
Preset^S	Clear^R	Clock	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\bar{Q}_0$

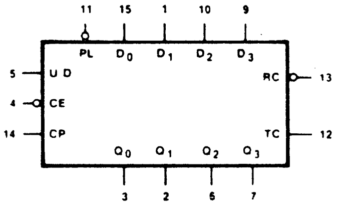
H = high level (steady state) L = low level (steady state)

*This condition is nonstable. It will not remain after clear and preset return to their inactive (high) state.

PRESETTABLE BCD/DECADE UP/DOWN COUNTER 74 SERIES "190"

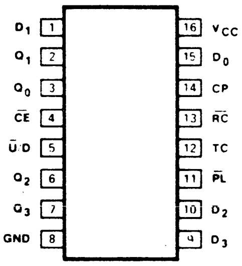
D-2024
D-2026
D-2027
D-2028

LOGIC SYMBOL


11
15
1
10
9
PL
D0
D1
D2
D3
5
U D
4
CE
14
CP
RC
13
TC
12
Q0
Q1
Q2
Q3
3
2
6
7

V_{CC} = Pin 16
GND = Pin 8

PIN CONFIGURATION


D1 1
Q1 2
Q0 3
CE 4
U/D 5
Q2 6
Q3 7
GND 8
16 VCC
15 D0
14 CP
13 RC
12 TC
11 PL
10 D2
9 D3

MODE SELECT-FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS
	$\overline{PL}$	$\overline{U}/D$	$\overline{CE}$	CP	D_n	Q_n
Parallel load	L	X	X	X	L	L
	L	X	X	X	H	H
Count up	H	L	l	↑	X	count up
Count down	H	H	l	↑	X	count down.
Hold "do nothing"	H	X	H	X	X	no change

TC AND $\overline{RC}$ TRUTH TABLE

INPUTS			TERMINAL COUNT STATE				OUTPUTS	
$\overline{U}/D$	$\overline{CE}$	CP	Q_0	Q_1	Q_2	Q_3	TC	$\overline{RC}$
H	X	X	H	X	X	H	L	H
L	H	X	H	X	X	H	H	H
L	L	⊔	H	X	X	H	H	⊔
L	X	X	L	L	L	L	L	H
H	H	X	L	L	L	L	H	H
H	L	⊔	L	L	L	L	H	⊔

H = HIGH voltage level steady state.
L = LOW voltage level steady state.
l = LOW voltage level one setup time prior to the LOW-to-HIGH clock transition.
X = Don't care
↑ = LOW-to-HIGH clock transition.
⊔ = LOW pulse.

QUAD 2-INPUT EXCLUSIVE-OR GATE 7486

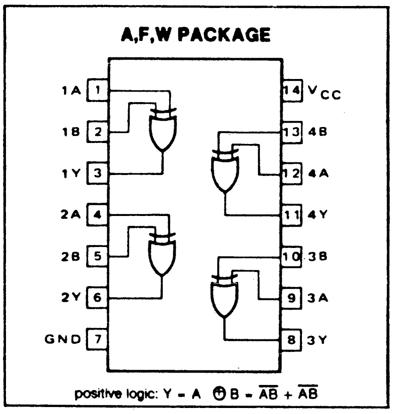
D-2029

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

H= high level, L = low level

PIN CONFIGURATION


A,F,W PACKAGE
1A
1B
1Y
2A
2B
2Y
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
Vcc
4B
4A
4Y
3B
3A
3Y
positive logic: Y = A ⊕ B = $\overline{A}B + A\overline{B}$

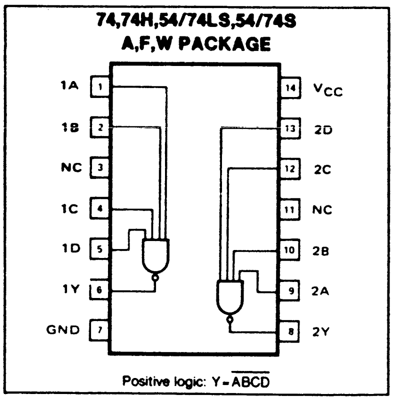
DUAL 4-INPUT NAND GATE 7420

D-2031

TRUTH TABLE

A	B	C	D	X
0	0	0	0	1
1	0	0	0	1
0	1	0	0	1
1	1	0	0	1
0	0	1	0	1
1	0	1	0	1
0	1	1	0	1
1	1	1	0	1
0	0	0	1	1
1	0	0	1	1
0	1	0	1	1
1	1	0	1	1
0	0	1	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	0

PIN CONFIGURATION


74,74H,54/74LS,54/74S
A,F,W PACKAGE
1A
1B
NC
1C
1D
1Y
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
Vcc
2D
2C
NC
2B
2A
2Y
Positive logic: Y = $\overline{ABCD}$

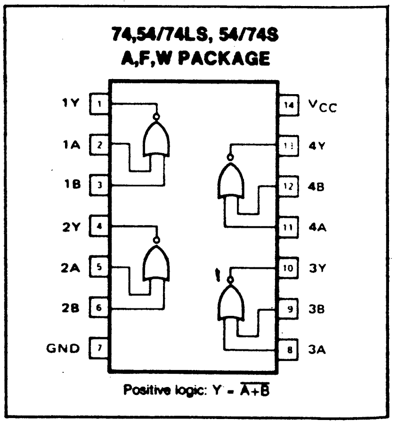
QUAD 2-INPUT NOR GATE 7402

D-2016
D-2032
D-2037

TRUTH TABLE

A	B	X
0	0	1
1	0	0
0	1	0
1	1	0

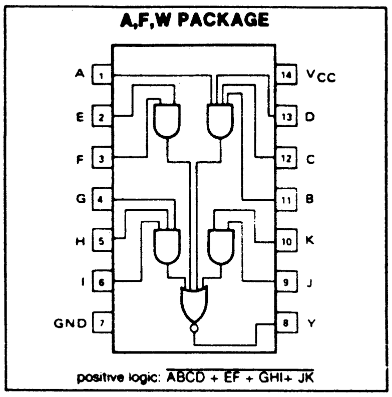
PIN CONFIGURATION


74,54/74LS, 54/74S
A,F,W PACKAGE
1Y
1A
1B
2Y
2A
2B
GND
1
2
3
4
5
6
7
14
13
12
11
10
9
8
Vcc
4Y
4B
4A
3Y
3B
3A
Positive logic: Y = $\overline{A+B}$

4-2-3-2-INPUT AND-OR GATE 7464

D-2033

PIN CONFIGURATION


A,F,W PACKAGE

A 1
E 2
F 3
G 4
H 5
I 6
GND 7
14 VCC
13 D
12 C
11 B
10 K
9 J
8 Y

positive logic: $\overline{ABCD + EF + GHI + JK}$

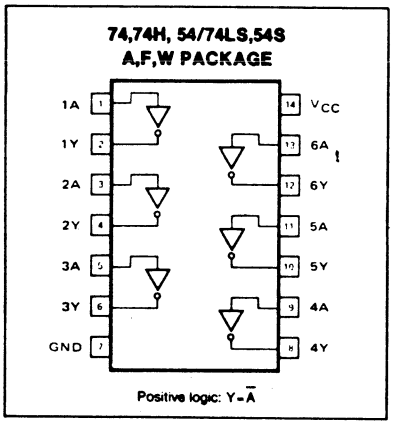
HEX INVERTER 7404

D-2039

TRUTH TABLE

A	Y
0	1
1	0

PIN CONFIGURATION


74,74H, 54/74LS,54S
A,F,W PACKAGE

1A 1
1Y 2
2A 3
2Y 4
3A 5
3Y 6
GND 7
14 VCC
13 6A
12 6Y
11 5A
10 5Y
9 4A
8 4Y

Positive logic: $Y=\overline{A}$

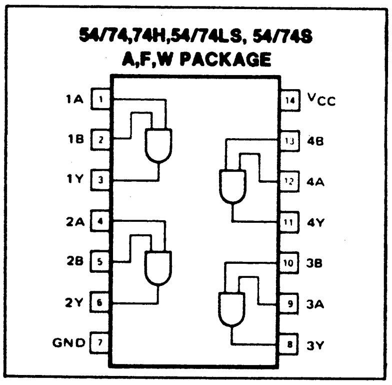
QUAD 2-INPUT AND GATE 7408

D-2051

TRUTH TABLE

A	B	X
0	0	0
1	0	0
0	1	0
1	1	1

PIN CONFIGURATION

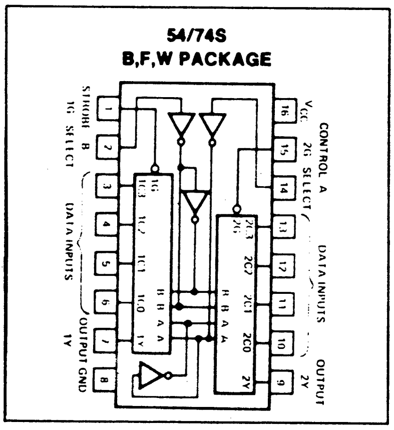

54/74,74H,54/74LS, 54/74S
A,F,W PACKAGE

1A 1
1B 2
1Y 3
2A 4
2B 5
2Y 6
GND 7
14 VCC
13 4B
12 4A
11 4Y
10 3B
9 3A
8 3Y

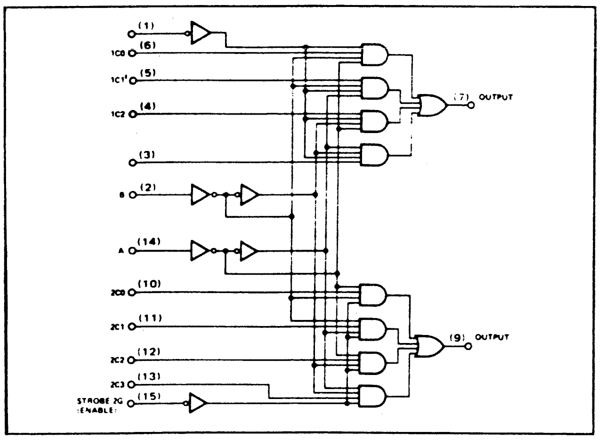
DUAL 4-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER 74253

D-2053
D-2054
D-2056
D-2057

PIN CONFIGURATION


54/74S
B,F,W PACKAGE
STROBE 1G
SELECT B
DATA INPUTS
OUTPUT 1Y
GND
VCC
CONTROL 2G
SELECT A
DATA INPUTS
OUTPUT 2Y
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9

BLOCK DIAGRAM


(1)
1C0 (6)
1C1 (5)
1C2 (4)
(3)
B (2)
A (14)
2C0 (10)
2C1 (11)
2C2 (12)
2C3 (13)
STROBE 2G (ENABLE) (15)
(7) OUTPUT
(9) OUTPUT

TRUTH TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level. L = low level. X = irrelevant. Z = high impedance (off)

FUNCTIONAL PIN DEFINITION (as used in the PM 3540) uP 8085

D2059

The following describes the function of the used pins.

AD_{0-7} (input/output 3-state)

Multiplexed Address/Data Bus: Lower 8-bits of the memory address (or I/O address) appear on the bus during the first clock pulse. It then becomes the data bus during the second and third clock pulse of each machine cycle.

3-stated during Hold and Halt modes.

A_1-A_{15} (Output 3-State)

Address Bus: The most significant 8-bits of the memory address.

ALE (Output 3-state)

Address Latch Enable: It occurs during the first clock pulse of each machine cycle and enables the address to get latched into the address fatch (D2062). The falling edge of ALE is set to guarantee setup and hold times for the address information.

CLK (Output)

Clock Output for use when a crystal network is used as an input to CPU.

READY (Input)

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

RESET IN (input)

Reset sets the Program Counter to zero. The CPU is held in the reset condition as long as Reset is applied.

RD (Output 3-state)

READ: indicates the selected memory or I/O position is to be read and that the Data Bus is available for the data transfer.

WR (Output 3-state)

WRITE: indicates the data on the Data Bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR.

SID (input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

V_{CC}

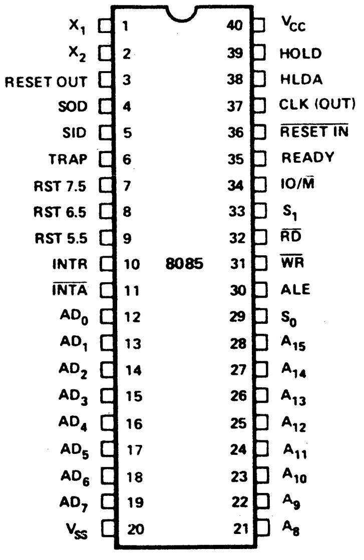
+5 volt supply.

V_{SS}

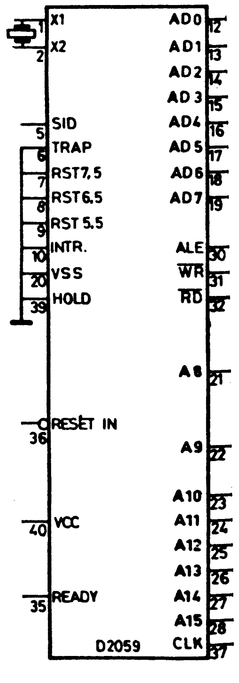
Ground Reference.

X_1, X_2 (input)

Crystal network connections to set the clock generator.


X1 1
X2 2
RESET OUT 3
SOD 4
SID 5
TRAP 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
INTR 10
INTA 11
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
VSS 20
8085
40 VCC
39 HOLD
38 HLDA
37 CLK (OUT)
36 RESET IN
35 READY
34 IO/M
33 S1
32 RD
31 WR
30 ALE
29 S0
28 A15
27 A14
26 A13
25 A12
24 A11
23 A10
22 A9
21 A8

8085 PINOUT DIAGRAM


1 X1
2 X2
5 SID
6 TRAP
7 RST7.5
8 RST6.5
9 RST 5.5
10 INTR.
20 VSS
39 HOLD
36 RESET IN
40 VCC
35 READY
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
ALE 30
WR 31
RD 32
A8 21
A9 22
A10 23
A11 24
A12 25
A13 26
A14 27
A15 28
CLK 37
D2059

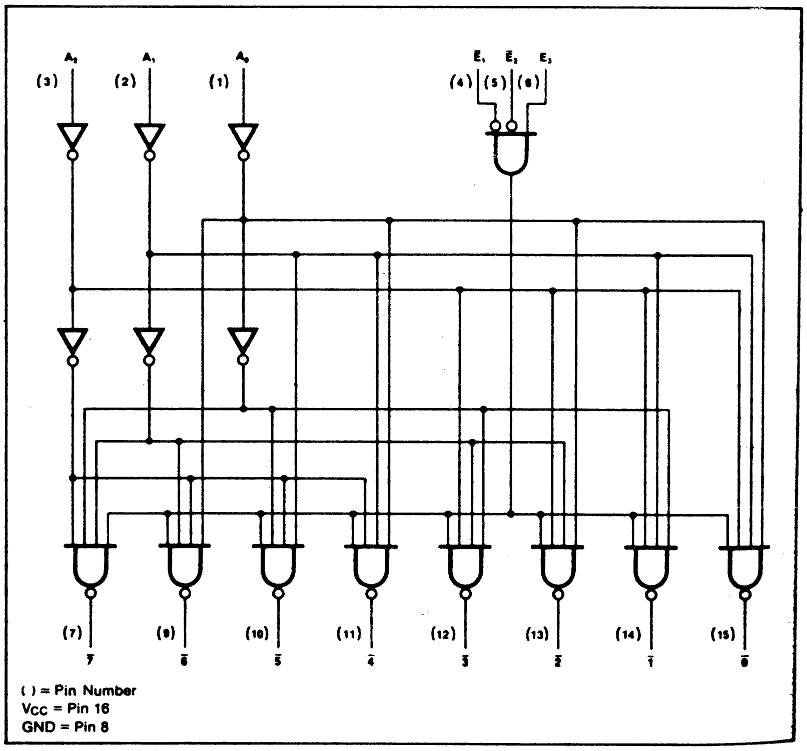
D-2061
D-2063

TRUTH TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{0}$	$\overline{1}$	$\overline{2}$	$\overline{3}$	$\overline{4}$	$\overline{5}$	$\overline{6}$	$\overline{7}$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

NOTES
H = HIGH voltage level
L = LOW voltage level
X = Don't care

LOGIC DIAGRAM

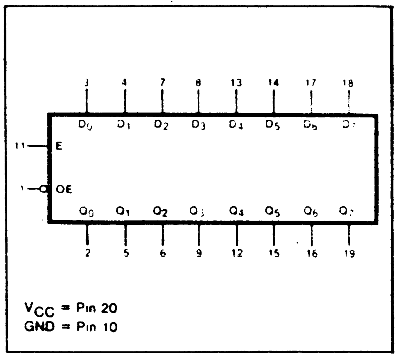

(3) A_2
(2) A_1
(1) A_0
(4) $\overline{E}_1$
(5) $\overline{E}_2$
(6) E_3
(7) $\overline{7}$
(9) $\overline{6}$
(10) $\overline{5}$
(11) $\overline{4}$
(12) $\overline{3}$
(13) $\overline{2}$
(14) $\overline{1}$
(15) $\overline{0}$

( ) = Pin Number
V_{CC} = Pin 16
GND = Pin 8

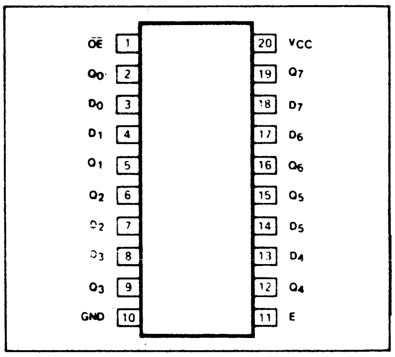
OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS 74 SERIES "373"

D-2062

LOGIC SYMBOL


3
4
7
8
13
14
17
18
D_0
D_1
D_2
D_3
D_4
D_5
D_6
D_7
11
E
1
OE
Q_0
Q_1
Q_2
Q_3
Q_4
Q_5
Q_6
Q_7
2
5
6
9
12
15
16
19
V_{CC} = Pin 20
GND = Pin 10

PIN CONFIGURATION

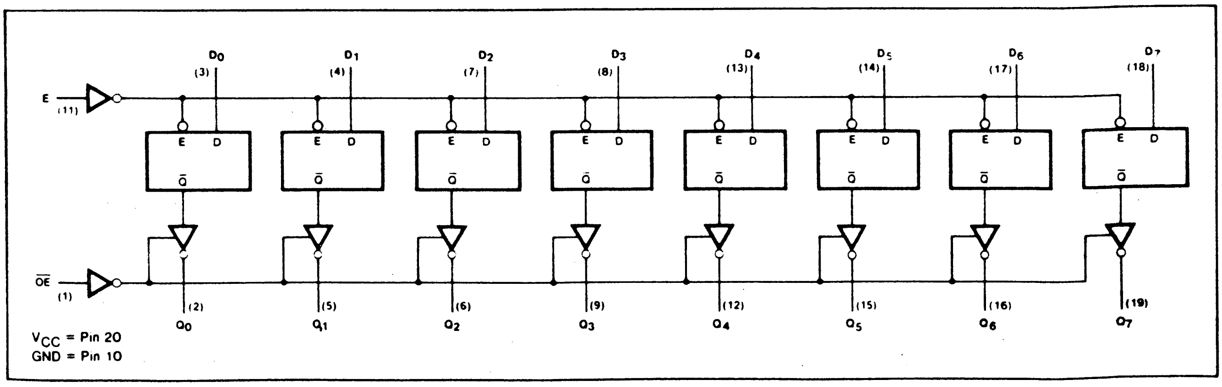

$\overline{OE}$ 1
Q_0 2
D_0 3
D_1 4
Q_1 5
Q_2 6
D_2 7
D_3 8
Q_3 9
GND 10
20 V_{CC}
19 Q_7
18 D_7
17 D_6
16 Q_6
15 Q_5
14 D_5
13 D_4
12 Q_4
11 E

MODE SELECT—FUNCTION TABLE

OPERATING MODES	INPUTS				OUTPUTS
	$\overline{OE}$	E	D_n	INTERNAL REGISTER	Q_0-Q_7
Enable & read register	L L	H H	L H	L H	L H
Latch & read register	L L	L L	l h	L H	L H
Latch register & disable outputs	H H	L L	l h	L H	(Z) (Z)

H = HIGH voltagel level
h = HIGH voltage one setup time prior to the HIGH-to-LOW enable transition
L = LOW voltage level
l = LOW voltage level one setup time prior to the HIGH-to-LOW enable transition
(Z) = High impedance "off" state

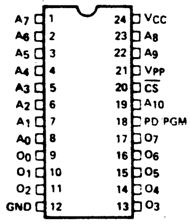
LOGIC DIAGRAM


E
(11)
$\overline{OE}$
(1)
D_0 (3)
D_1 (4)
D_2 (7)
D_3 (8)
D_4 (13)
D_5 (14)
D_6 (17)
D_7 (18)
E
D
$\bar{Q}$
(2) Q_0
(5) Q_1
(6) Q_2
(9) Q_3
(12) Q_4
(15) Q_5
(16) Q_6
(19) Q_7
V_{CC} = Pin 20
GND = Pin 10

D-2064A
D-2064B
D-2076

16K (2K×8) UV ERASABLE PROM 2716

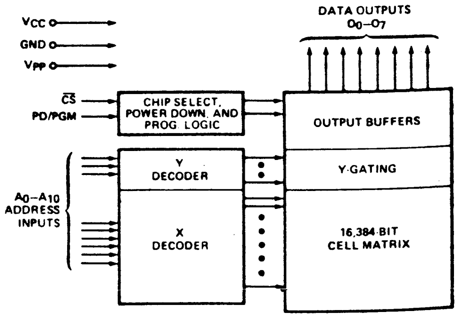
PIN CONFIGURATION


A7 1
A6 2
A5 3
A4 4
A3 5
A2 6
A1 7
A0 8
O0 9
O1 10
O2 11
GND 12
24 VCC
23 A8
22 A9
21 VPP
20 $\overline{CS}$
19 A10
18 PD PGM
17 O7
16 O6
15 O5
14 O4
13 O3

MODE SELECTION

MODE \ PINS	PD/PGM (18)	$\overline{CS}$ (20)	V_{PP} (21)	V_{CC} (24)	OUTPUTS (9-11, 13-17)
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Deselect	Don't Care	V_{IH}	+5	+5	High Z
Power Down	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

BLOCK DIAGRAM


DATA OUTPUTS
O0–O7
VCC
GND
VPP
$\overline{CS}$
PD/PGM
CHIP SELECT, POWER DOWN, AND PROG. LOGIC
OUTPUT BUFFERS
Y DECODER
Y GATING
A0–A10 ADDRESS INPUTS
X DECODER
16,384-BIT CELL MATRIX

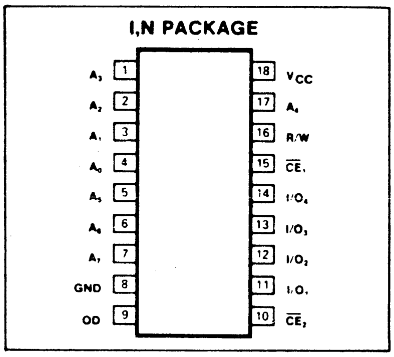
PIN NAMES

A0–A10	ADDRESSES
PD/PGM	POWER DOWN/PROGRAM
$\overline{CS}$	CHIP SELECT
O0–O7	OUTPUTS

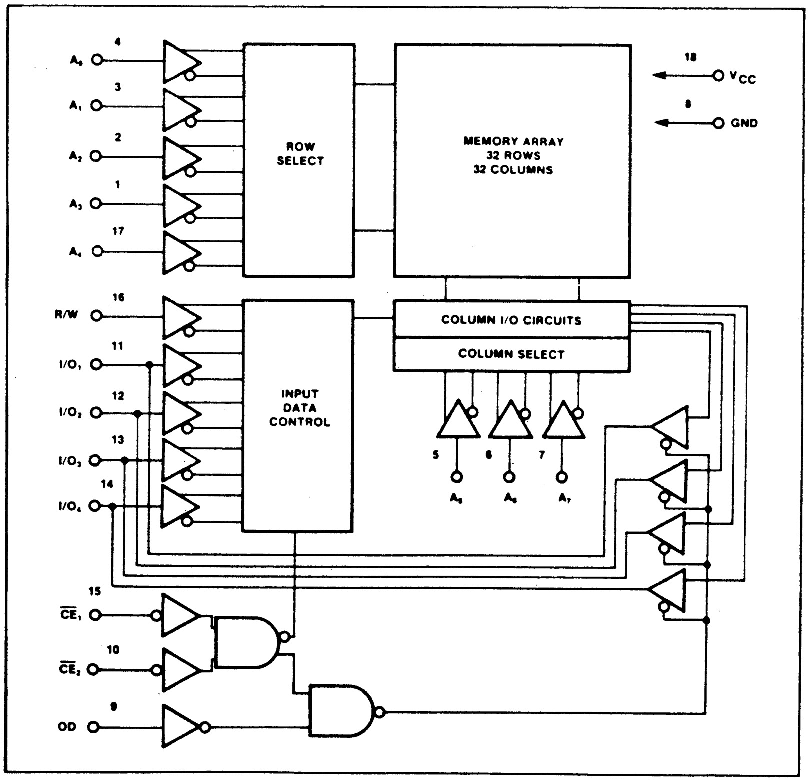
1024-BIT STATIC MOS RAM (256X4) Am 9111

D-2067
D-2068

PIN CONFIGURATION

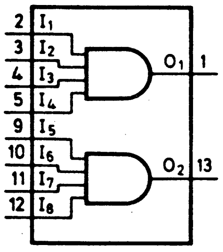

I,N PACKAGE
A3 1
A2 2
A1 3
A0 4
A5 5
A6 6
A7 7
GND 8
OD 9
18 VCC
17 A4
16 R/W
15 CE1
14 I/O4
13 I/O3
12 I/O2
11 I/O1
10 CE2

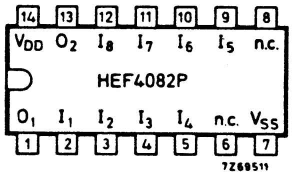
BLOCK DIAGRAM


A0 4
A1 3
A2 2
A3 1
A4 17
R/W 16
I/O1 11
I/O2 12
I/O3 13
I/O4 14
CE1 15
CE2 10
OD 9
ROW SELECT
MEMORY ARRAY 32 ROWS 32 COLUMNS
18 VCC
8 GND
COLUMN I/O CIRCUITS
COLUMN SELECT
INPUT DATA CONTROL
5 A5
6 A6
7 A7

SYNCHRONOUS UP/DOWN COUNTER, BINARY/DECADE COUNTER HEF4029P

D-2058


2 I1
3 I2
4 I3
5 I4
9 I5
10 I6
11 I7
12 I8
O1 1
O2 13
7Z69570

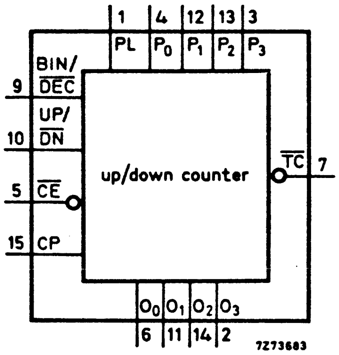

14 13 12 11 10 9 8
VDD O2 I8 I7 I6 I5 n.c.
HEF4082P
O1 I1 I2 I3 I4 n.c. VSS
1 2 3 4 5 6 7
7Z69511

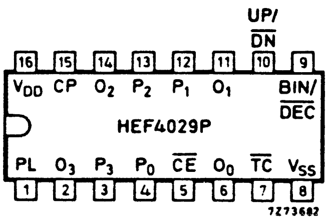
GENERAL DESCRIPTION

The HEF4082P provides the positive dual 4-input AND function. The outputs are fully buffered for highest noise immunity and pattern insensitivity of output impedance.

DUAL 4-INPUT AND GATE HEF4082P

D-2072
D-2073


1 4 12 13 3
PL P0 P1 P2 P3
BIN/DEC 9
UP/DN 10
CE 5
CP 15
up/down counter
TC 7
O0 O1 O2 O3
6 11 14 2
7Z73683


UP/DN
16 15 14 13 12 11 10 9
VDD CP O2 P2 P1 O1 BIN/DEC
HEF4029P
PL O3 P3 P0 CE O0 TC VSS
1 2 3 4 5 6 7 8
7Z73682

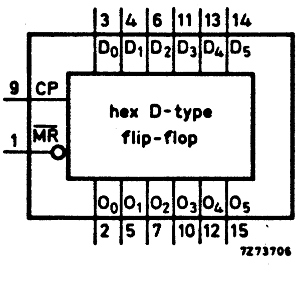
GENERAL DESCRIPTION

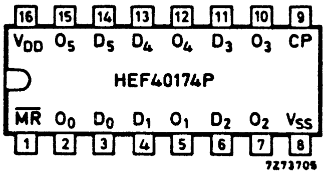
The HEF4029P is a synchronous edge-triggered up/down 4-bit binary/BCD decade counter with a clock input (CP), an active LOW count enable input ($\overline{CE}$), an up/down control input (UP/$\overline{DN}$), a binary/decade control input (BIN/$\overline{DEC}$), an overriding asynchronous active HIGH parallel load input (PL), four parallel data inputs (P_0 to P_3), four parallel buffered outputs (O_0 to O_3) and an active LOW terminal count output ($\overline{TC}$).

Information on P_0 to P_3 is loaded into the counter while PL is HIGH, independent of all other input conditions. With PL LOW, operation is synchronous and is edge-triggered on the LOW-to-HIGH transition of CP. Operation is determined by the three synchronous mode control inputs; UP/$\overline{DN}$, BIN/$\overline{DEC}$ and $\overline{CE}$.
These inputs must be stable only during the set-up time prior to the LOW-to-HIGH transition of CP and the hold time after this clock transition.
$\overline{TC}$ is LOW when the counter is at its terminal count, as determined by the counting mode, and $\overline{CE}$ is LOW.

HEX D-TYPE FLIP-FLOP HEF4017P

D-2074
D-2078
D-2079


3 4 6 11 13 14
D0 D1 D2 D3 D4 D5
9 CP
1 MR
hex D-type flip-flop
O0 O1 O2 O3 O4 O5
2 5 7 10 12 15
7Z73706


16 15 14 13 12 11 10 9
VDD O5 D5 D4 O4 D3 O3 CP
HEF40174P
MR O0 D0 D1 O1 D2 O2 VSS
1 2 3 4 5 6 7 8
7Z73705

GENERAL DESCRIPTION

The HEF40174P is a hex edge-triggered D-type flip-flop with six data inputs (D_0 to D_5), a clock input (CP) an overriding asynchronous master reset input ($\overline{MR}$), and six buffered outputs (O_0 to O_5).
Information on D_0 to D_5 is transferred to O_0 to O_5 on the LOW-to-HIGH transition of CP if $\overline{MR}$ is HIGH. When LOW, $\overline{MR}$ resets all flip-flops (O_0 to O_5 = LOW) independent of CP and D_0 to D_5.

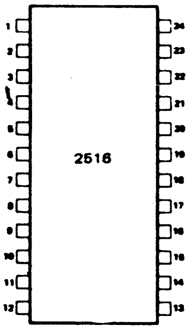
64X6X8 STATIC CHARACTER GENERATOR 2516

D-2076

SILICON GATE MOS 2500 SERIES

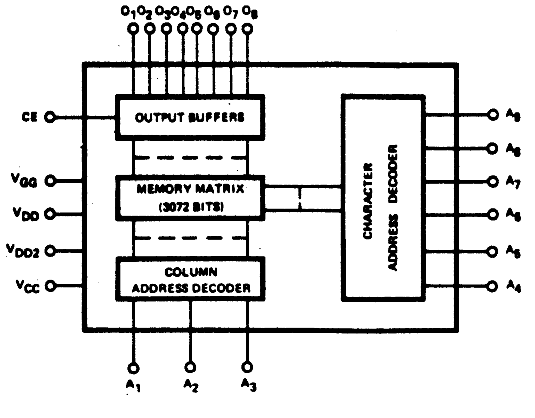
PIN CONFIGURATION **(Top View)**

N/I PACKAGES


2516
1
2
3
4
5
6
7
8
9
10
11
12
24
23
22
21
20
19
18
17
16
15
14
13

1. Chip Enable	24. V_{CC}
2. NC	23. V_{GG}
3. Output 8	22. Address 9
4. Output 7	21. Address 8
5. Output 6	20. Address 7
6. Output 5	19. Address 6
7. Output 4	18. Address 5
8. Output 3	17. Address 4
9. Output 2	16. Address 3
10. Output 1	15. Address 2
11. Ground	14. Address 1
12. V_{DD}	13. NC

BLOCK DIAGRAM

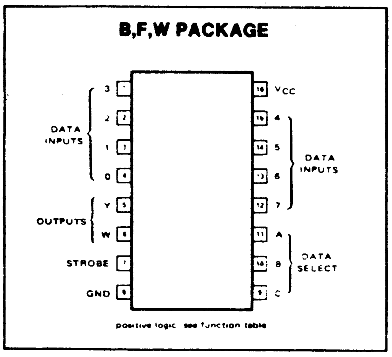

O1 O2 O3 O4 O5 O6 O7 O8
CE
VGG
VDD
VDD2
VCC
OUTPUT BUFFERS
MEMORY MATRIX (3072 BITS)
COLUMN ADDRESS DECODER
CHARACTER ADDRESS DECODER
A9
A8
A7
A6
A5
A4
A1
A2
A3

CE	OUTPUT
0	DATA
1	OPEN

8-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER 74151

D-2077

PIN CONFIGURATION


B,F,W PACKAGE
DATA INPUTS
3
2
1
0
OUTPUTS
Y
W
STROBE
GND
1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
VCC
4
5
6
7
DATA INPUTS
A
B
C
DATA SELECT
positive logic: see function table

TRUTH TABLE

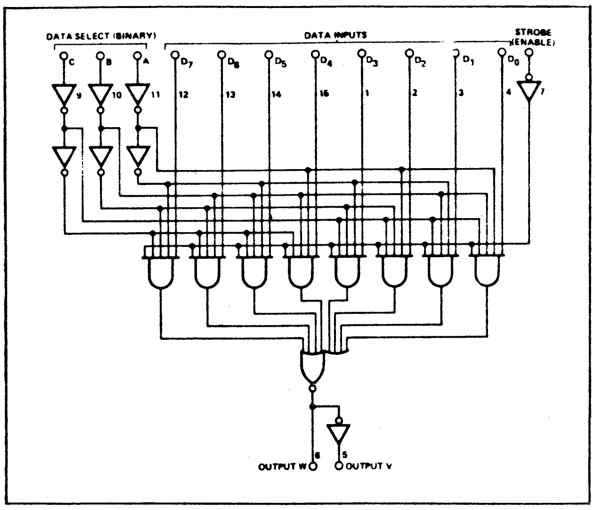
INPUTS				OUTPUTS	
SELECT			STROBE		
C	B	A	S	Y	W
X	X	X	H	L	H
L	L	L	L	D0	$\overline{D0}$
L	L	H	L	D1	$\overline{D1}$
L	H	L	L	D2	$\overline{D2}$
L	H	H	L	D3	$\overline{D3}$
H	L	L	L	D4	$\overline{D4}$
H	L	H	L	D5	$\overline{D5}$
H	H	L	L	D6	$\overline{D6}$
H	H	H	L	D7	$\overline{D7}$

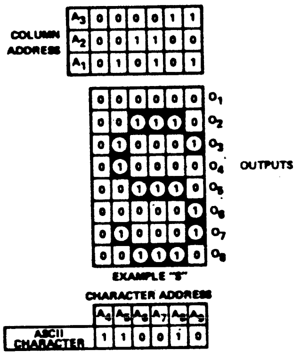
H = high level, L = low level, X = irrelevant
D0, D1 . . . D7 = the level of the D respective input

SPEED/PACKAGE AVAILABILITY

54	F,W	74	B,F
54LS	F,W	74LS	B,F
54S	F,W	74S	B,F

BLOCK DIAGRAM

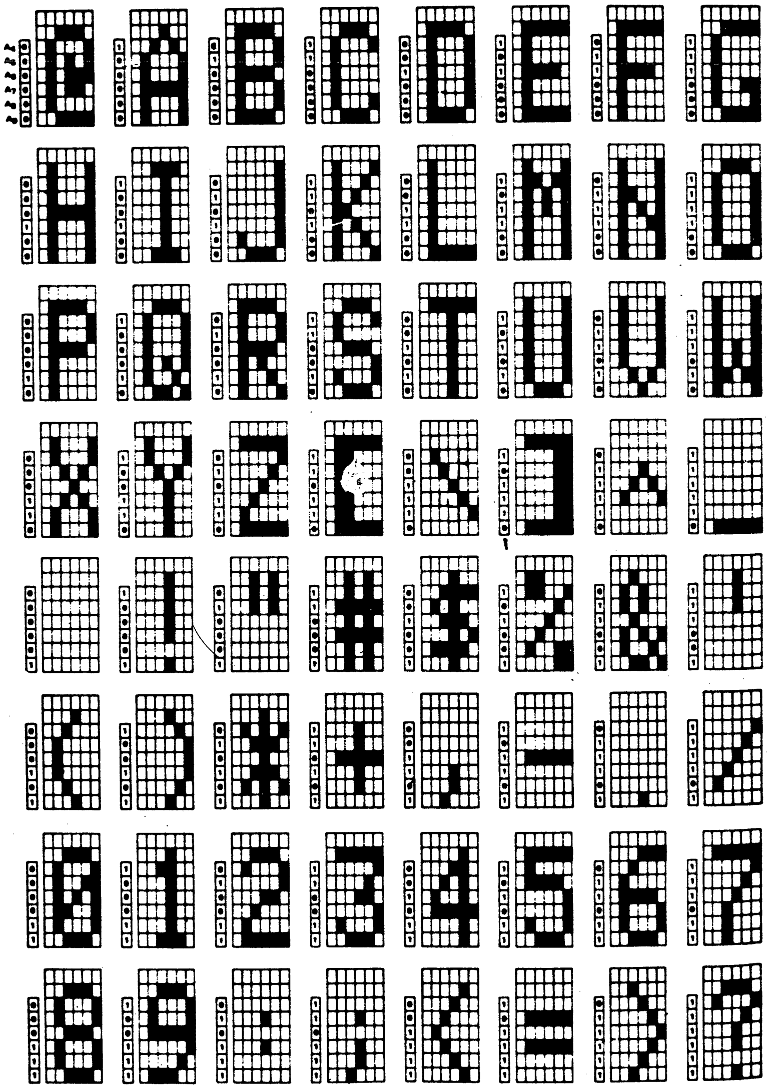

DATA SELECT (BINARY)
C
B
A
DATA INPUTS
D_7
D_6
D_5
D_4
D_3
D_2
D_1
D_0
STROBE (ENABLE)
9
10
11
12
13
14
15
1
2
3
4
7
6
5
OUTPUT W
OUTPUT Y


COLUMN ADDRESS
A3
A2
A1
O1
O2
O3
O4
O5
O6
O7
O8
OUTPUTS
EXAMPLE "S"
CHARACTER ADDRESS
ASCII CHARACTER

NOTE:
Undefined (column) addresses result in "1" level (high) outputs.

SIGNETICS 64 X 6 X 8 STATIC CHARACTER GENERATOR ■ 2516

ASCII CHARACTER FONT



NOTE: Excess addresses yield logic "1" outputs.

CODING SYSTEM OF FAILURE REPORTING FOR QUALITY ASSESSMENT OF T & M INSTRUMENTS

(excl. potentiometric recorders)

The information contents of the coded failure description is necessary for our computerized processing of quality data.

Since the reporting of repair and maintenance routines must be complete and exact, we give you an example of a correctly filled-out PHILIPS SERVICE Job sheet.

① Country	② Day Month Year	③ Typenumber /Version	④ Factory/Serial no.
32	150475	OPM326002	DO00783

CODED FAILURE DESCRIPTION ⑥

⑤ *Nature of call*	*Location*	*Component/sequence no.*	*Category*
☐ Installation		TS0607	5
☐ Pre sale repair		R00631	2
☐ Preventive maintenance	0021	990001	4
☒ Corrective maintenance			
☐ Other			

⑦ *Job completed* ☒

Working time ⑧ ☐☐12 Hrs

Detailed description of the information to be entered in the various boxes:

①Country: 32 = Switzerland

②Day Month Year 150475 = 15 April 1975

③Type number/Version OPM326002 = Oscilloscope PM 3260, version 02 (in later oscilloscopes this number is placed in front of the serial no)

④Factory/Serial number DO00783 = DO 783 These data are mentioned on the type plate of the instrument

⑤Nature of call: Enter a cross in the relevant box

⑥Coded failure description

Location

☐☐☐☐

These four boxes are used to isolate the problem area. Write the code of the part in which the fault occurs, e.g. unit no or mechanical item no of this part (refer to 'PARTS LISTS' in the manual).

Example: 0001 for Unit 1
000A for Unit A
0075 for item 75

If units are not numbered, do not fill in the four boxes; see Example Job sheet.

Component/sequence no.

☐☐☐☐☐☐

These six boxes are intended to pinpoint the faulty component.

A. Enter the component designation as used in the circuit diagram. If the designation is alfa-numeric, the letters must be written (starting from the left) in the two left-hand boxes and the figures must be written (in such a way that the last digit occupies the right-most box) in the four right-hand boxes.

B. Parts not identified in the circuit diagram:

990000	Unknown/Not applicable
990001	Cabinet or rack (text plate, emblem, grip, rail, graticule, etc.)
990002	Knob (incl. dial knob, cap, etc.)
990003	Probe (only if attached to instrument)
990004	Leads and associated plugs
990005	Holder (valve, transistor, fuse, board, etc.)
990006	Complete unit (p.w. board, h.t. unit, etc.)
990007	Accessory (only those without type number)
990008	Documentation (manual, supplement, etc.)
990009	Foreign object
990099	Miscellaneous

Category

☐

0 Unknown, not applicable (fault not present, intermittent or disappeared)
1 Software error
2 Readjustment
3 Electrical repair (wiring, solder joint, etc.)
4 Mechanical repair (polishing, filing, remachining, etc.)
5 Replacement (of transistor, resistor, etc.)
6 Cleaning and/or lubrication
7 Operator error
8 Missing items (on pre-sale test)
9 Environmental requirements are not met

⑦Job completed: Enter a cross when the job has been completed.

⑧Working time: Enter the total number of working hours spent in connection with the job (excluding travelling, waiting time, etc.), using the last box for tenths of hours.

☐☐12 = 1,2 working hours (1 h 12 min.)

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telex Mi 35290

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tel. 2393811/353533

Zaire: Philips S.Z.R.L., B.P. 1798, Kinshasa;
tel. 31208

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Professional Equipment Division, P.O.B. 553;
Kitwe; tel. 2526/7/8

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Eindhoven - The Netherlands

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